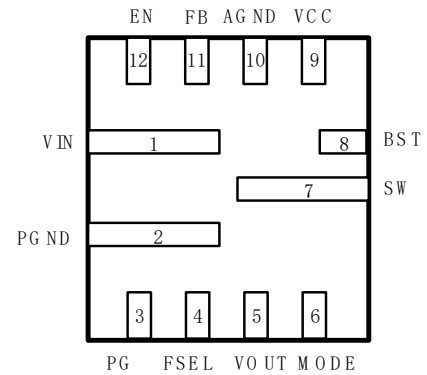


SCT2360

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL

Over operating free-air temperature unless otherwise noted ⁽¹⁾

DESCRIPTION	MIN	MAX	UNIT
VIN, EN	-0.3	32	V
SW	-1	32	V
BST	-0.3	38	V
BST-SW	-0.3	6	V
VOUT	-0.3	16	V
PG, FSEL, MODE, VCC, FB	-0.3	6	V
Operating junction temperature ⁽²⁾	-40	125	C
Storage temperature T _{STG}	-65	150	C



Top View: FCUTQFN3*3-12L, Plastic

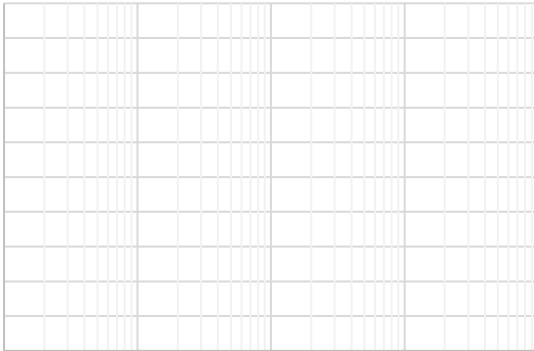
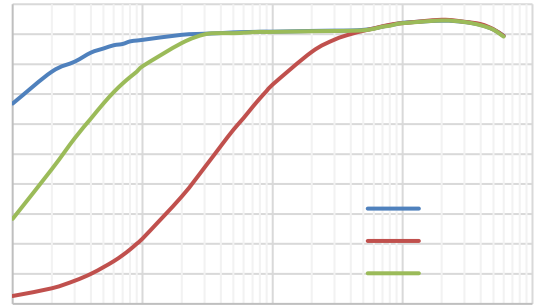
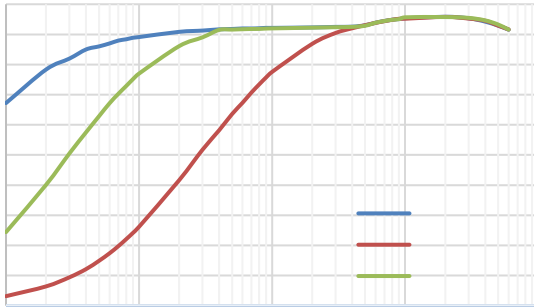
(1)

(2)

NAME	NO.	PIN FUNCTION
VIN	1	Input voltage. Decouple the input rail with at least 0.1uF input ceramic capacitor. Place the capacitor as close to VIN and PGND pins as possible. Use wide PCB traces and multiple vias to make the connection.
PGND	2	Power ground. Using wide PCB traces and multiple vias large enough to handle the load current.
PG	3	Power good open-drain output. PG is high if the output voltage is higher than 95% and lower than 105% of the nominal voltage.
FSEL	4	Switching frequency selection. Connecting to ground sets clock frequency to 400KHz. Floating sets clock frequency to 800KHz. Connecting to VCC sets clock frequency to 1.2MHz.
VOUT	5	VOUT is used to sense the output voltage of the buck regulator. Connect VOUT to the output capacitor of the regulator directly. Keep the VOUT sensing trace far away from the SW node. VIAs should also be avoided on the VOUT sensing trace. A trace larger than 25mil is required.
MODE	6	PFM, USM or FCCM mode selection. Connect the pin to VCC to force the device in Forced Continuous Current Modulation (FCCM) operation mode. Ground the pin to operate the device in Pulse Frequency Modulation (PFM) mode without Ultrasonic Mode (USM). Floating the pin to operate the device in PFM with USM.

SCT2360

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
	Protection					



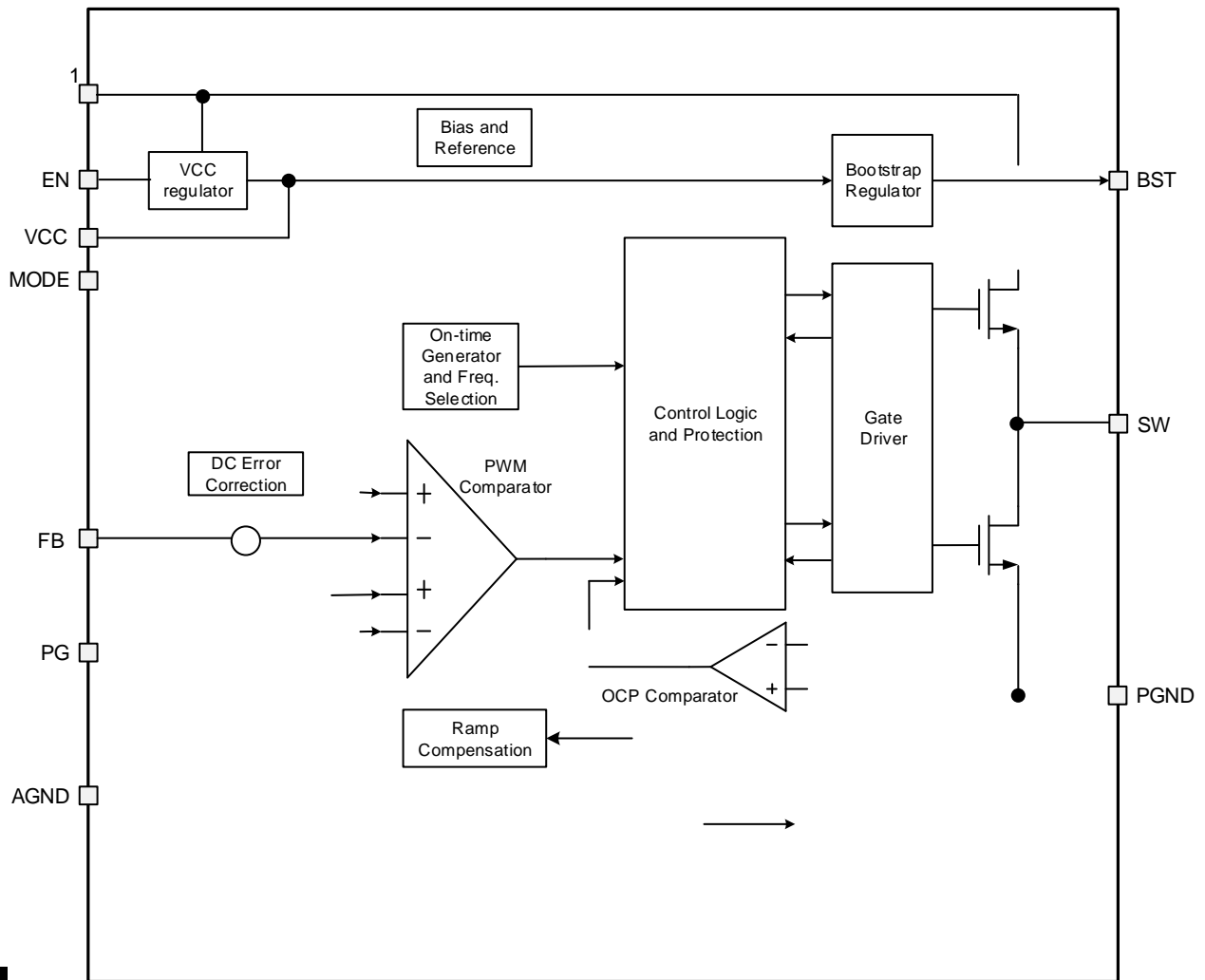


Figure 7. Functional Block Diagram

Overview

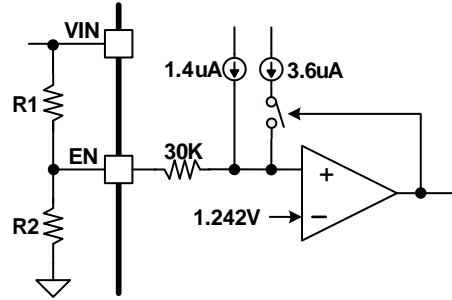
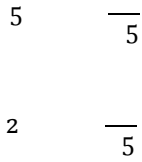
Constant on-time (COT) Mode Control

Pulse Frequency Modulation (PFM) and Ultra-sonic Modulation (USM) Modes

Forced Pulse Width Modulation (FPWM) mode

SCT2360

Enable and Under Voltage Lockout Threshold



Output Voltage



Internal Soft-Start

Switching Frequency Selection

Table 1. FSEL Pin Set-up for Switching Frequency Selection

Mode Selection

Table 2. MODE Pin Set-up for Mode Selection

Power Good (PG)

Bootstrap Voltage Regulator

Over Current Limit and Hiccup Mode

Under-voltage Protection

SCT2360

Over voltage Protection

Thermal Shutdown

Typical Application

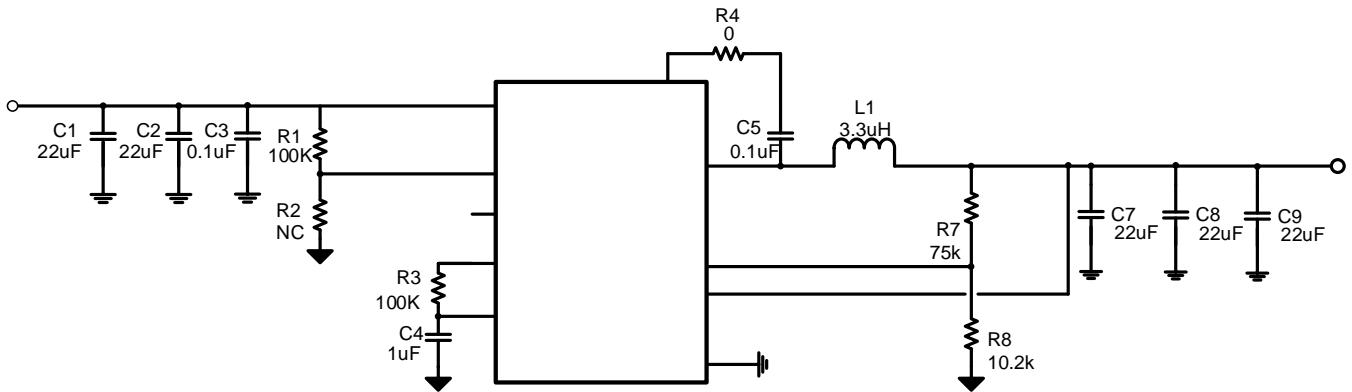


Figure 9. 12V Input, 5V/6A Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V
Output Voltage	5V
Output Current	6A
Output voltage ripple (peak to peak)	50mV
Switching Frequency	400kHz

SCT2360

Input Capacitor Selection

Output Capacitor Selection

1

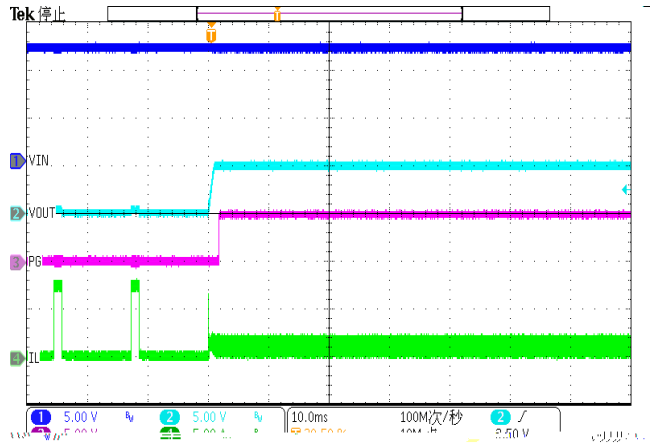
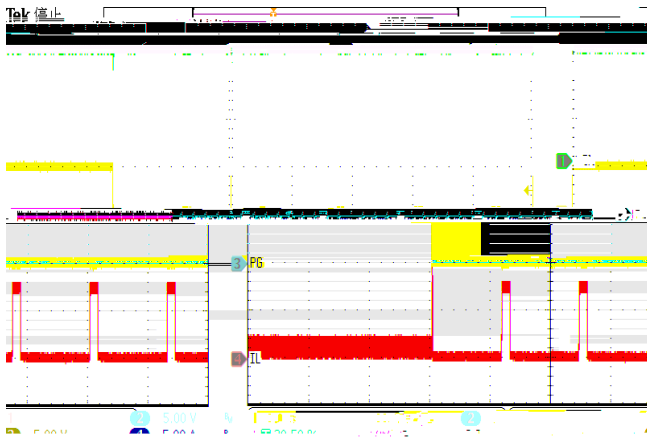
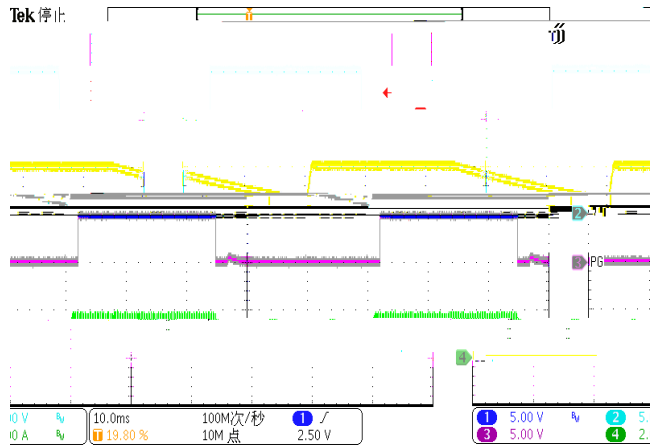
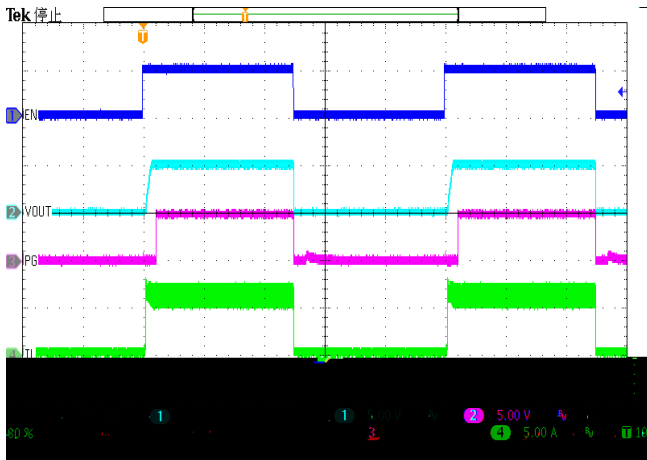
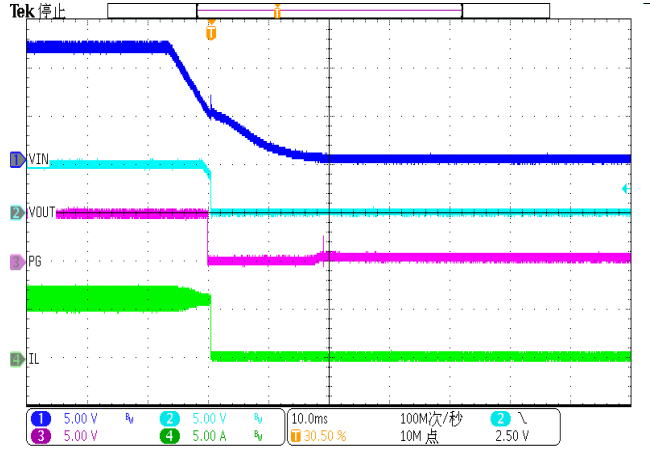
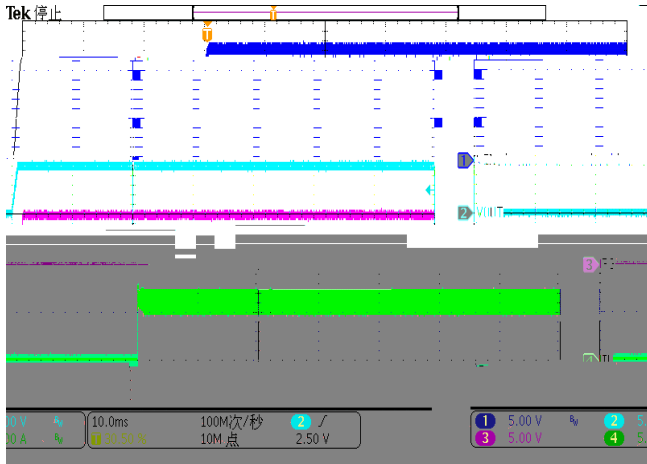
Output Feedback Resistor Divider Selection

Table 3. Recommended Component Values for Typical Output Voltage (Vin=12V)

F _{sw} (kHz)	Vout (V)	L (uH)	R7 (k)	R8 (k)	Cout(uF)

SCT2360

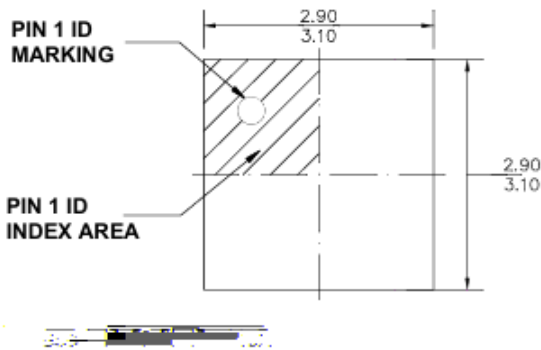
Application Waveforms(continued)



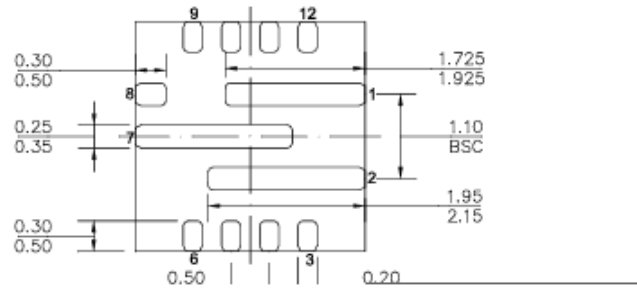
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Sayonora

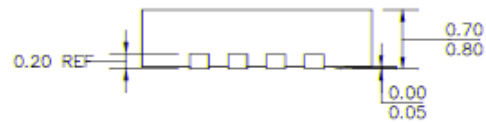
- 1.
2. PFP KQER QHURDHROD.PP/RR' HUHADQ @UE
- 3.



BOTTOM VIEW



TOP VIEW



SIDE VIEW

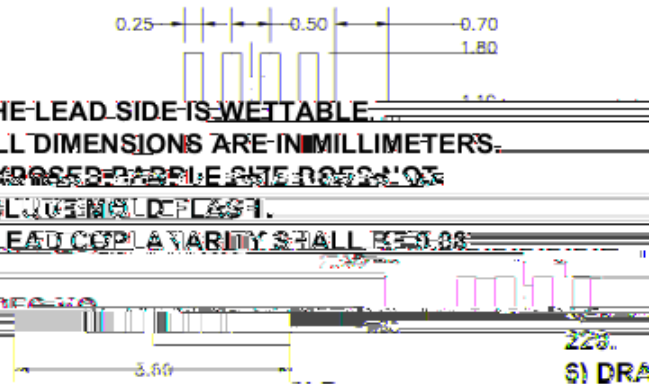
NOTE:

- 1) THE LEAD SIDE IS WETTABLE.
- 2) ALL DIMENSIONS ARE IN MILLIMETERS.
- 3) EXPOSED PALLE SITE DOES NOT INCLUDE MOLD FLASH.
- 4) LEAD COPLANARITY SHALL BE 0.08

MILLIMETERS MAX.

PLACING CONFIRMS TO JESD609

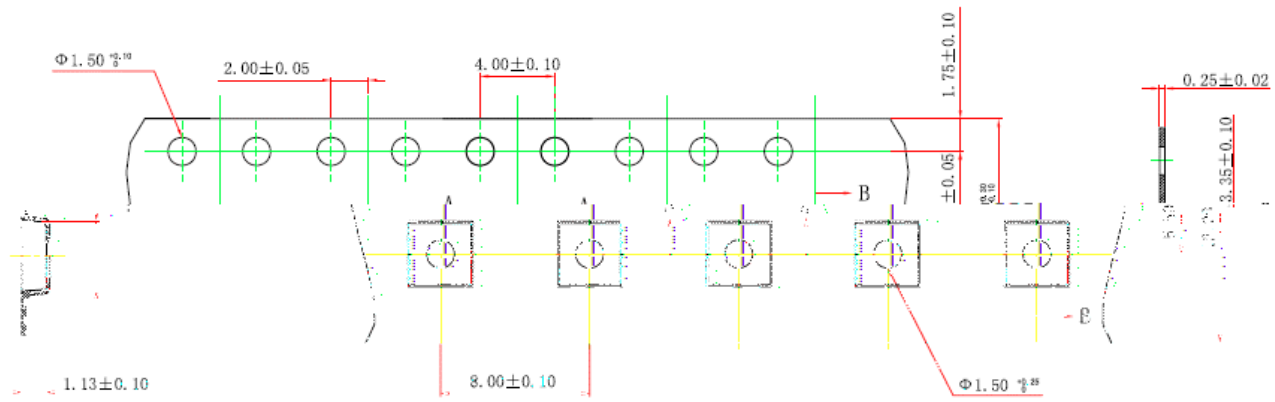
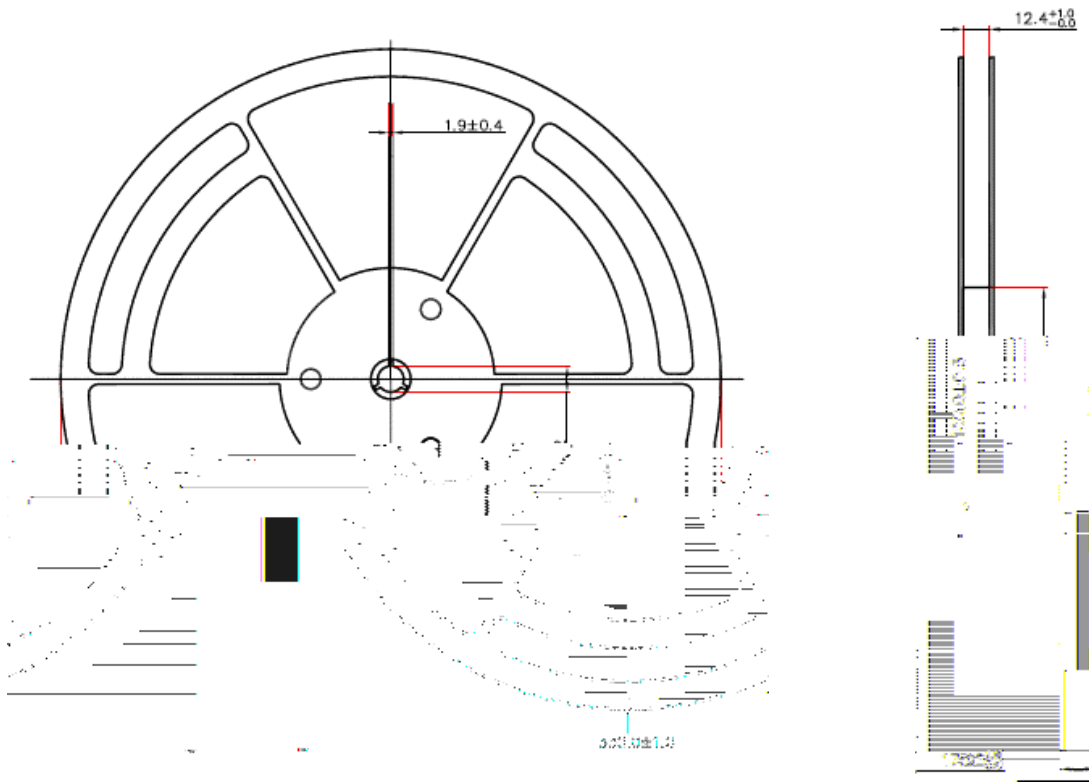
VIEWING IS NOT TO SCALE.



5) DRAWING

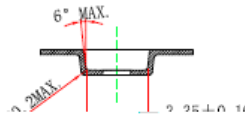
RECOMMENDED LAND PATTERN

SCT2360



SECTION B-B

SECTION A-A



SECTION A-A

SECTION B-B