



# SCT2131Q

## REVISION HISTORY

Revision 0.8: Customer sample.

## DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DESCRIPTION
SCT2131QFTA	131Q	QFN-8L1.5mm*2mm

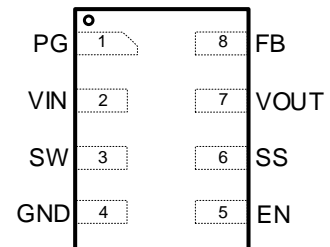
1) For Tape & Reel, Add Suffix R (e.g., SCT2131QFTAR)

## ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature unless otherwise noted <sup>(1)</sup>

DESCRIPTION	MIN	MAX	UNIT
VIN, EN, PG, SW, VOUT	-0.3	7	V
SS, FB	-0.3	5.5	V
Operating junction temperature T <sub>J</sub> <sup>(2)</sup>	-40	150	C
Storage temperature T <sub>STG</sub>	-65	150	C

## PIN CONFIGURATION



Top View: QFN-8L 1.5mm x 2mm, Plastic

(1)

(2)

## PIN FUNCTIONS

Pin	Function	
PG	1	
VIN	2	
SW	3	Switch output. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time.
GND	4	
EN	5	Enable logic input.
SS	6	
VOUT	7	
FB	8	



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## ELECTRICAL CHARACTERISTICS

$V_{IN}=5V$ ,  $T_J=-40^{\circ}C\sim 125^{\circ}C$ , typical values are tested under  $25^{\circ}C$ .

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
<b>Power Supply and Output</b>						
$V_{IN}$	Operating input voltage		2.8		6	V
$V_{IN\_UVLO}$	Input UVLO	$V_{IN}$ rising		2.7		V
	Hysteresis			175		mV
$I_{SD}$	Shutdown current			0		

TYPICAL CHARACTERISTICS

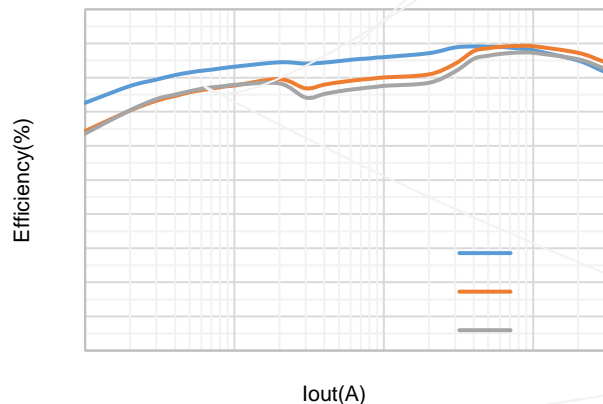


Figure 1. Efficiency vs Load Current,  $V_{out}=1.2V$

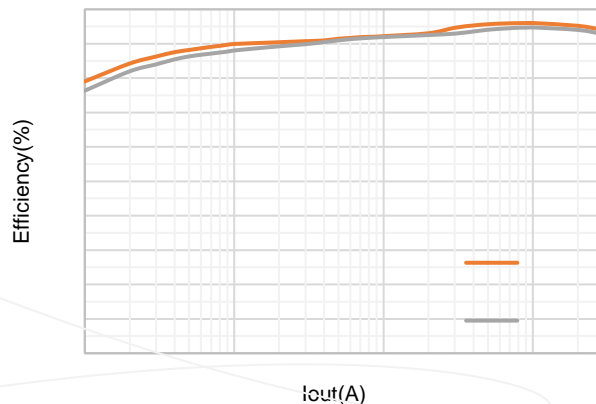


Figure 2. Efficiency vs Load Current,  $V_{out}=3.3V$

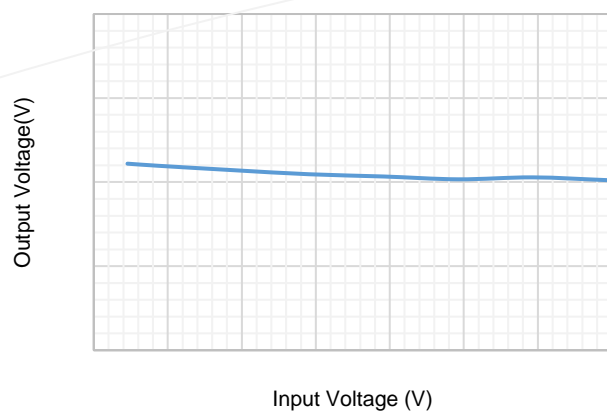


Figure 3. Line Regulation,  $I_o=1.5A$



Figure 4. Load Regulation,  $V_{in}=5V$

Figure 5.  $V_{FB}$  vs Temperature

Figure 6. UVLO vs Temperature

## FUNCTIONAL BLOCK DIAGRAM

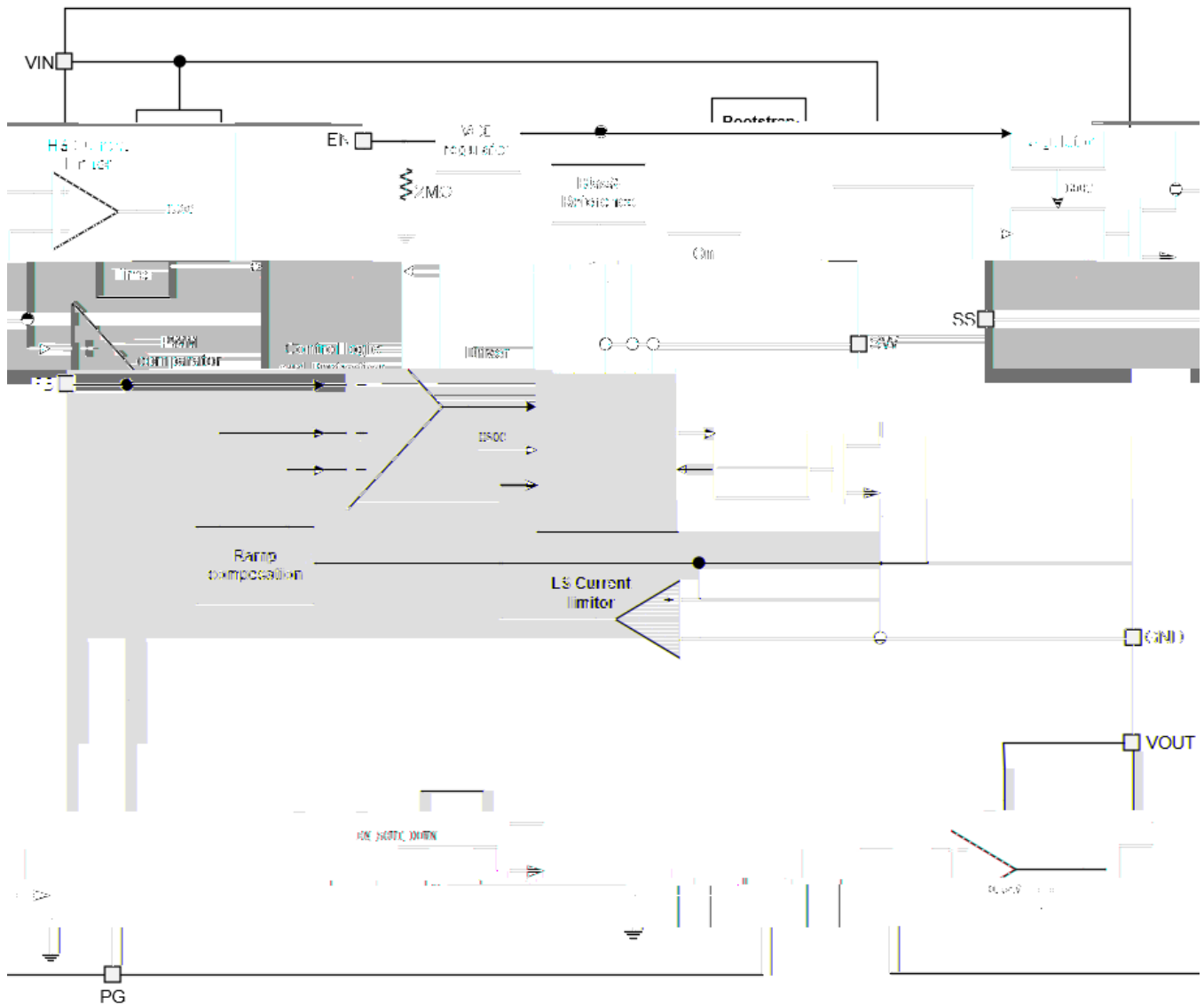


Figure 7. Functional Block Diagram

## OPERATION

### Overview

The SCT2131Q is a 2.8V-6V input, 3A output, synchronous buck converter with built-in 25mΩ high-side and 20mΩ R<sub>ds(on)</sub> low-side power MOSFETs. It implements constant on time control to regulate output voltage, providing excellent line and load transient response, and internal error amplifier integrated improve the line and load regulation.

The switching frequency is fixed 2.1MHz. The SCT2131Q features programmable soft start time to avoid large inrush current and output voltage overshoot during startup. The device also supports monolithic startup with pre-biased output condition. The SCT2131Q operates in Pulse Frequency Modulation (PFM) to improve low light load efficiency. The quiescent current is typically 65uA under no load and no switching.

The SCT2131Q full protection features include the input under-voltage lockout, over current protection with cycle-by-cycle current limiting and hiccup mode, output hard short protection and thermal shutdown protection.

### Constant On-time Control

Constant on-time (COT) control is employed to provide fast transient response and easy loop stabilization. At the beginning of each cycle, the high-side MOSFET is turned on for a fixed one

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When the device is disabled, the part automatically goes into output discharge mode, and its internal discharge MOSFET in VOUT pin provides a discharge path for the output capacitor.

## Output Voltage

The SCT2131Q regulates the internal reference voltage at 0.6V. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 2 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

$$\text{---} \tag{2}$$

Where:

- $R_{FB\_TOP}$  is the resistor connecting the output to the FB pin.
- $R_{FB\_BOT}$  is the resistor connecting the FB pin to the ground.

## Soft Start (SS)

The SCT2131Q has an external soft start (SS) pin that ramps up the output voltage at a controlled slew rate to the SS capacitor.  $t_{ss}$  can be calculated with Equation 3:

$$\text{---} \tag{3}$$

Where:

- $C_{ss}$  is the external SS capacitor.
- $I_{ss}$

The minimum SS capacitor is recommended to be 1nF.

## Over Current Protection (OCP) and Hiccup Mode

In each switching cycle, the inductor current is sensed by monitoring the high-side MOSFET during the ON period and the low-side MOSFET during the OFF period. When the inductor current ( $I_L$ ) reaches the high-side MOSFET peak current limit (typically 4.5A) during the ON period, the high-side MOSFET is forced off immediately to prevent the current from rising further. Then the low-side MOSFET turns on and stays on until  $I_L$  drops below the low-side MOSFET valley current limit (typically 3.5A). If output loading continues to increase, output will drop below the  $V_{UVP}$ , and SS pin is discharged such that output is 0V. Then the device will count for 7 cycles of soft-start time for hiccup -start period. If overload or hard short condition still exists during soft-start and make FB voltage lower than  $V_{UVP}$ , the device enters turning-off mode again. When overload or hard short condition is removed, the device automatically recovers to enters normal regulating operation.

## Power Good Indicator

The SCT2131Q has one power good (PG) output to indicate normal operation after the soft-start time. PG is the open drain of an internal MOSFET, which has a maximum  $R_{DS(ON)}$  below 2  $\Omega$  IN or an external voltage source through an external a resistor (e.g., MOSFET turns on, and PG is pulled to GND before soft start is ready. After  $V_{FB}$  reaches 95% of  $V_{REF}$ , PG is pulled high by the external voltage source with 80us delay. When  $V_{FB}$  drops to 90% or rises to 110% of  $V_{REF}$ , the PG

voltage is pulled to GND to indicate an output failure. If VIN and EN are not available, and PG is pulled up by an external power supply, PG will self-  
-up resistor is used, the voltage on the pin is below 0.4V.

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## APPLICATION INFORMATION

### Typical Application

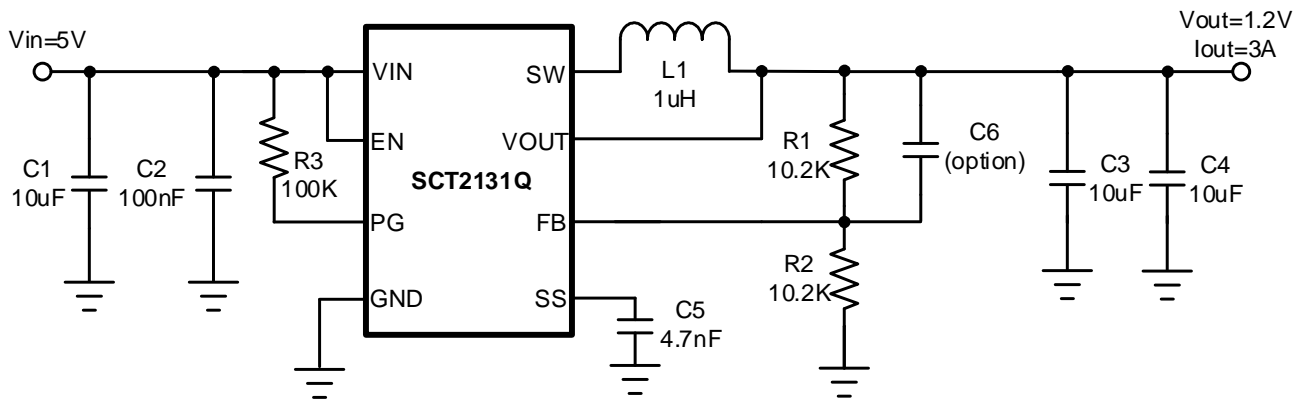


Figure 8. SCT2131Q Design Example, 1.2V Output

#### Design Parameters

Design Parameters	Example Value
Input Voltage	5V Normal 2.8V to 6V
Output Voltage	1.2V
Maximum Output Current	3A
Switching Frequency	2.1MHz
Output voltage ripple (peak to peak)	2mV
Transient Response 0.3A to 2.7A load step	Vout =140mV

## Output Voltage

The output voltage is set by an external resistor divider R1 and R2 in typical application schematic. Recommended R2 resistance is 10.2K . Use Equation 4 to calculate R1.

Table 1. R<sub>1</sub>, R<sub>2</sub> Value for Common Output Voltage (Room Temperature)

V <sub>OUT</sub>	R <sub>1</sub>	R <sub>2</sub>
1.2 V	10.2	10.2
1.8 V	20	10.2
3.3 V	46.5	10.2

$$\text{---} \quad (4)$$

where:

- V<sub>REF</sub> is the feedback reference voltage, typical 0.6V

## Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance (DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always corresponds to a bigger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductance to use is to allow the inductor peak-to-peak ripple current to be approximately 10%~40% of the maximum output current.

The peak-to-peak ripple current in the inductor I<sub>LPP</sub> can be calculated as in Equation 5.

$$\text{---} \quad (5)$$

Where:

- I<sub>LPP</sub> is the inductor peak-to-peak current.
- L is the inductance of inductor.
- f<sub>sw</sub> is the switching frequency.
- V<sub>OUT</sub> is the output voltage.
- V<sub>IN</sub> is the input voltage.

Since the inductor-current ripple increases with the input voltage, so the maximum input voltage in application is always used to calculate the minimum inductance required. Use Equation 6 to calculate the inductance value.

$$\text{---} \quad (6)$$

Where

- L<sub>MIN</sub> is the minimum inductance required.
- f<sub>sw</sub> is the switching frequency.
- V<sub>OUT</sub> is the output voltage.
- V<sub>IN(max)</sub> is the maximum input voltage.
- I<sub>OUT(max)</sub> is the maximum DC load current.
- LIR is coefficient of I<sub>LPP</sub> to I<sub>OUT</sub>.

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I<sub>LPEAK</sub> and I<sub>LRMS</sub> can be calculated as in Equation 7 and Equation 8.





## Application Waveforms

$V_{IN}=5V$ ,  $V_{OUT}=1.2V$ , unless otherwise noted

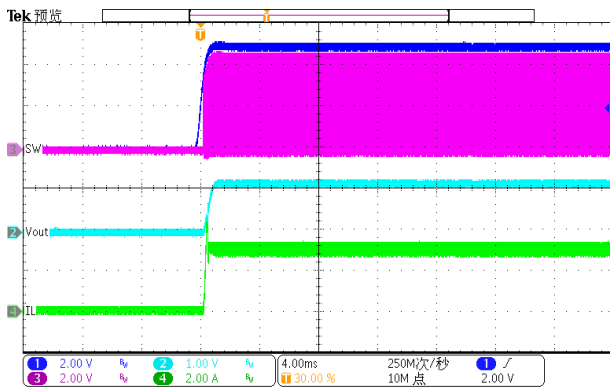


Figure 9. Power up ( $I_{LOAD}=3A$ )

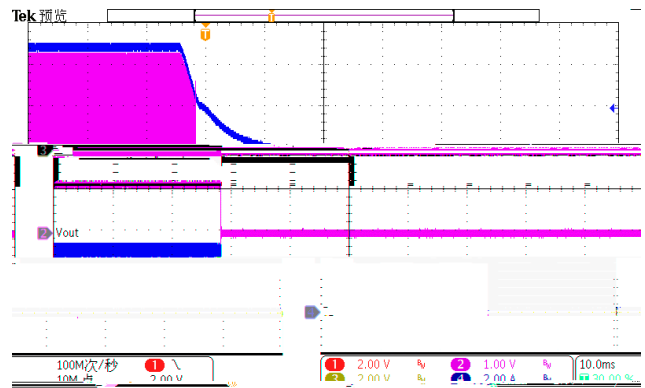


Figure 10. Power down ( $I_{LOAD}=3A$ )

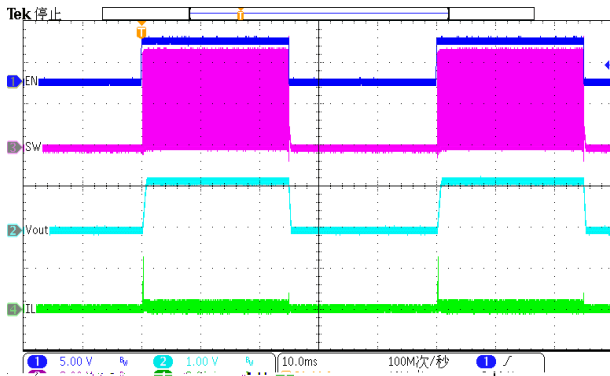


Figure 11. EN toggle ( $I_{LOAD}=0.1A$ )

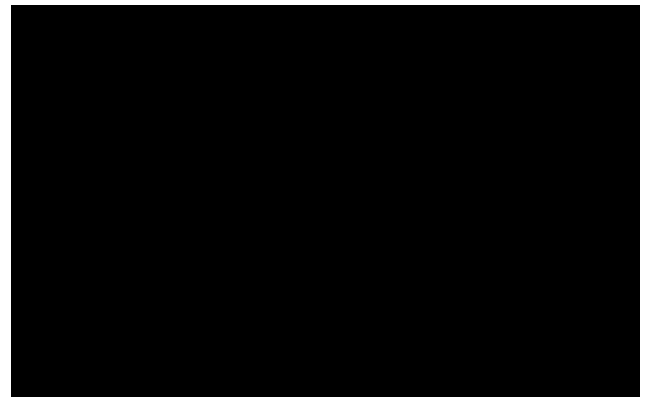


Figure 12. EN toggle ( $I_{LOAD}=3A$ )

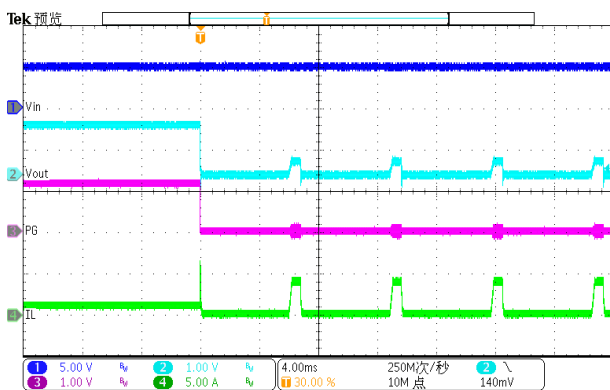


Figure 13. Over Current Protection (1A to hard short)

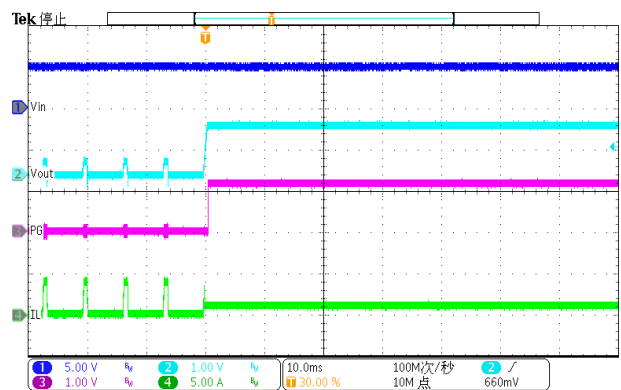


Figure 14. Over Current Release (hard short to 1A)

## Application Waveforms



Figure 15. Load Transient (0.3A-2.7A, 1.6A/us)

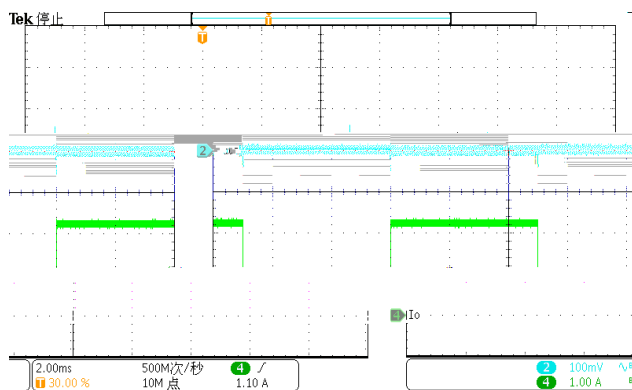


Figure 16. Load Transient (0.75A-2.25A, 1.6A/us)

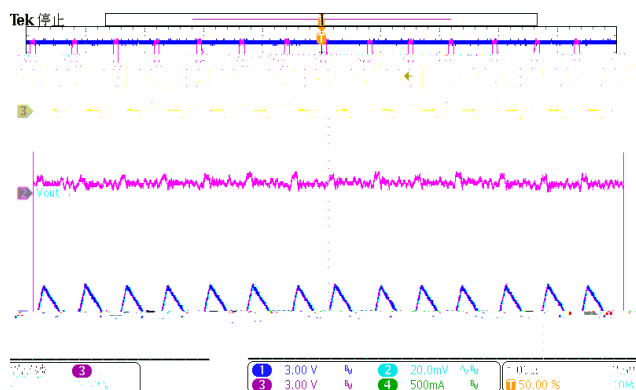


Figure 17. Output Ripple ( $I_{LOAD}=100mA$ )

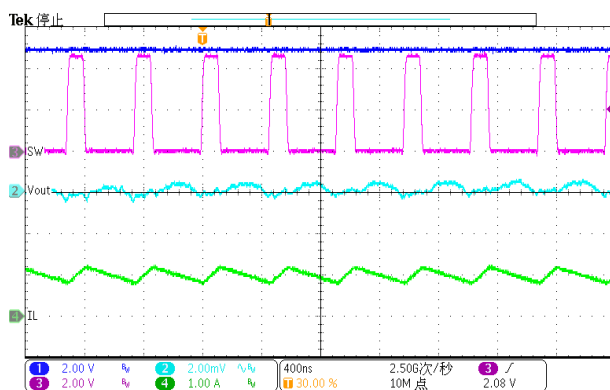


Figure 18. Output Ripple ( $I_{LOAD}=1A$ )

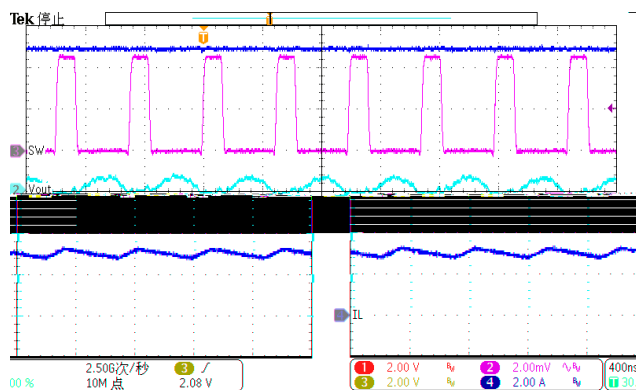


Figure 19. Output Ripple ( $I_{LOAD}=3A$ )

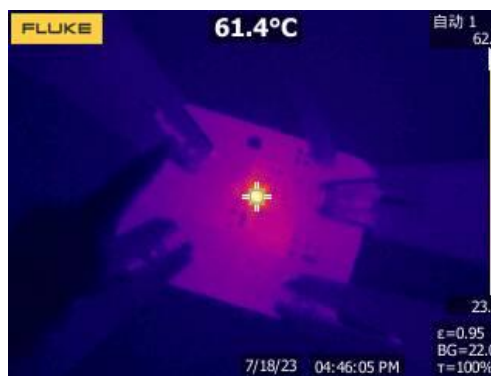


Figure 20. Thermal,  $V_{IN}=5V$ ,  $V_{OUT}=1.2V$ ,  $I_{LOAD}=3A$

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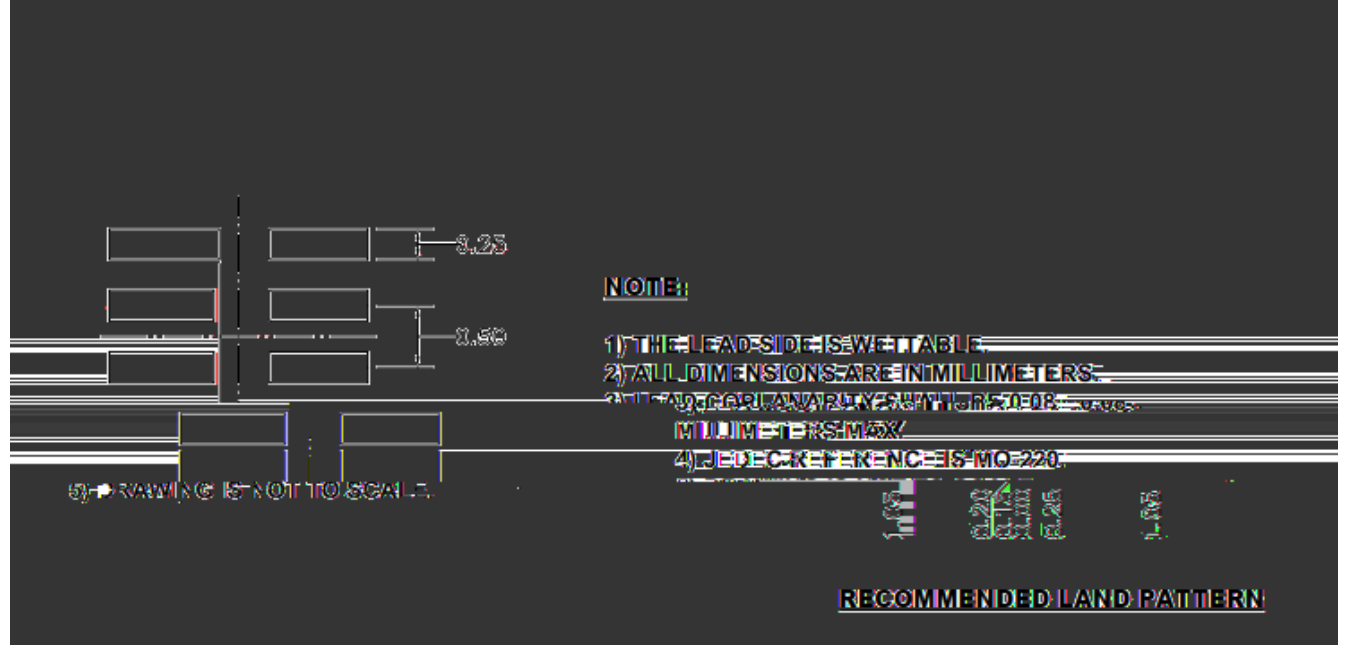
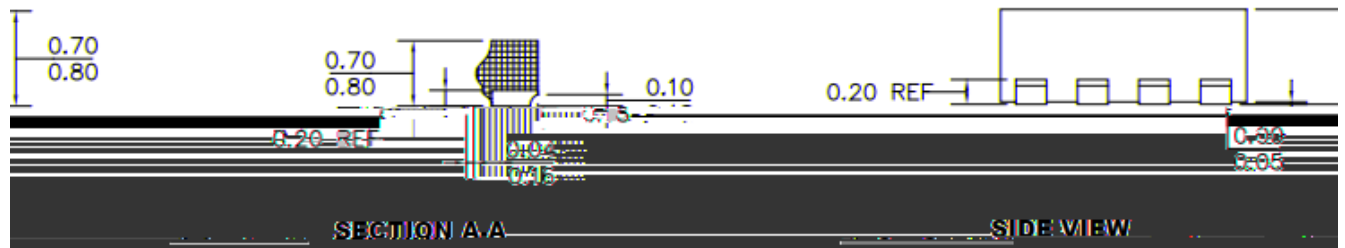
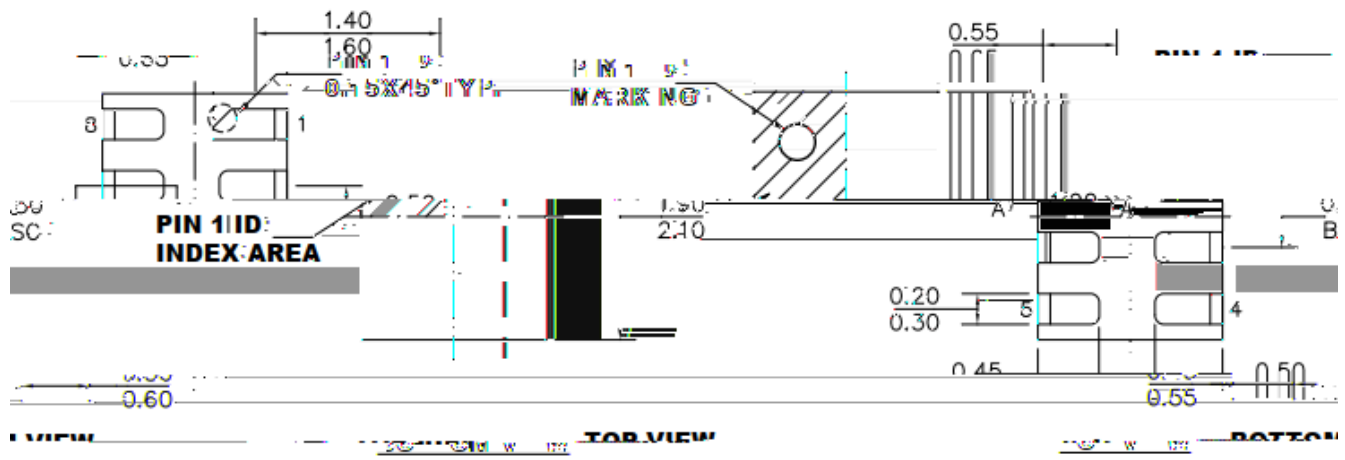
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## Layout Guideline

Proper PCB layout is a critical for SCT2131Q . The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impedance and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing overheat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impedance of grounding.
4. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground plane PCB plan

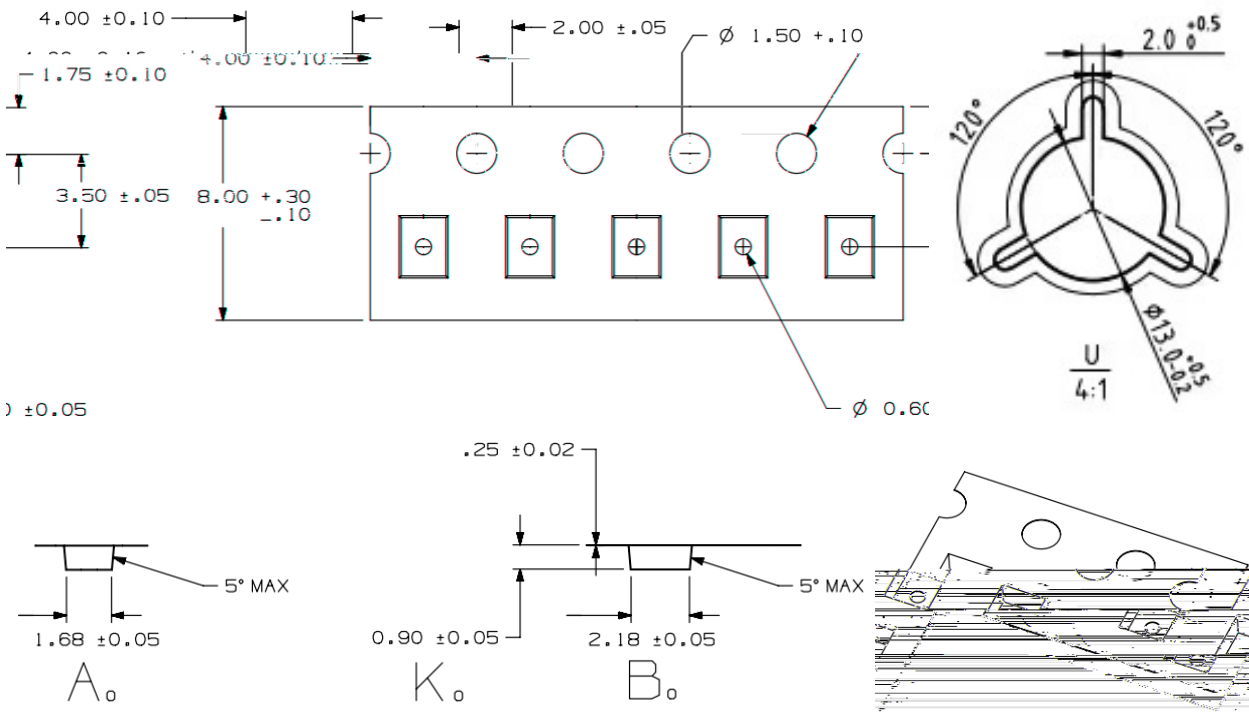
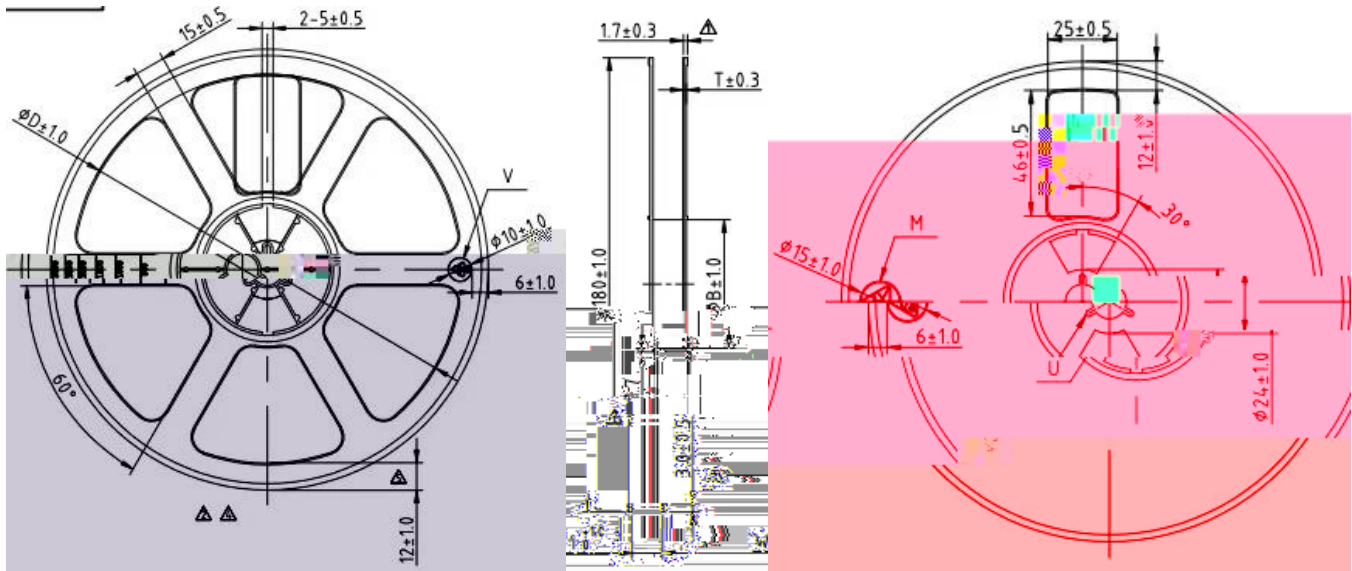
PACKAGE INFORMATION



# SCT2131Q

## TAPE AND REEL INFORMATION

Orderable Device	Package Type	Pins	SPQ
SCT2131QFTAR	QFN 1.5mmx2mm	8	3000



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