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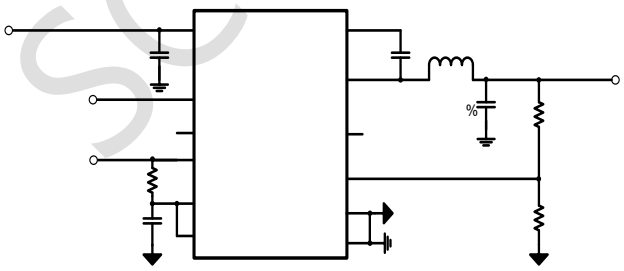
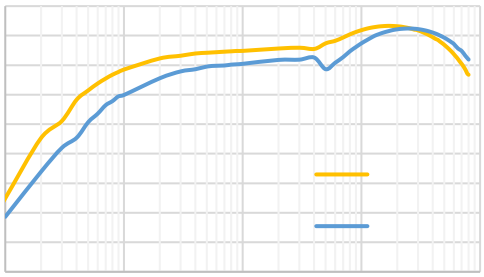
The SCT2161Q adopts a Constant On-Time (COT) control to provide fast transient response and easy loop stabilization. The switching clock frequency is fixed 2.2MHz for optimization of the filter size and output voltage ripple. The device offers fixed 1ms soft start to prevent inrush current during the startup of output voltage ramping. Power Good with open drain output signals that the output voltage is within regulation.

The SCT2161Q has the MODE pin to select Pulse Frequency Modulation (PFM) operation mode to achieve the light load power save, or Ultrasonic Mode (USM) to keep the switching frequency above audible frequency areas during light-load or no-load conditions, or Forced Continuous Conduction Mode (FCCM) to achieve the small output ripple.





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		Feedback voltage Input. Connect FB to the tap of a resistor divider from output voltage to AGND to set up output voltage. The device regulates FB to the internal reference value of 0.6V typical.

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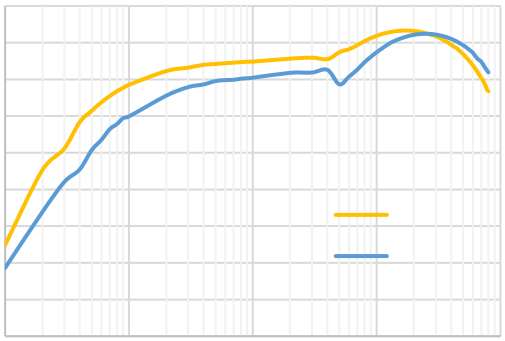

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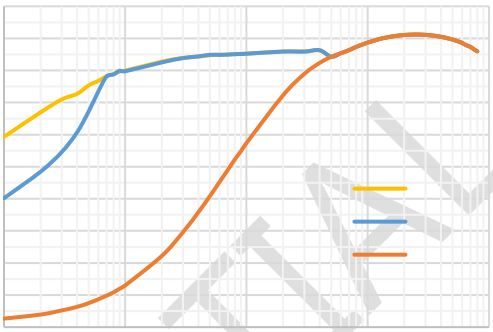

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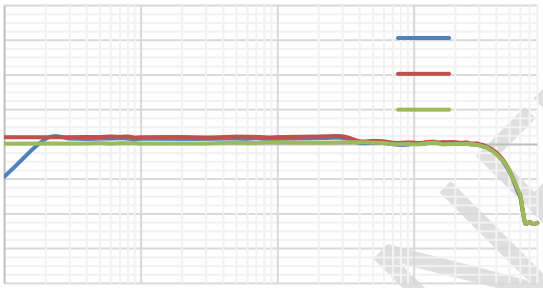

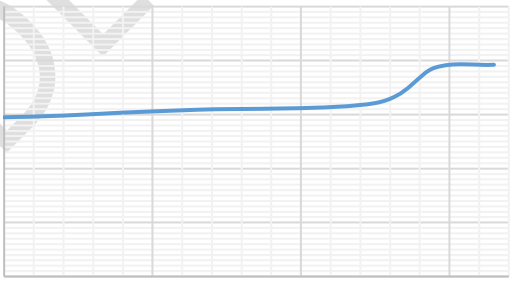

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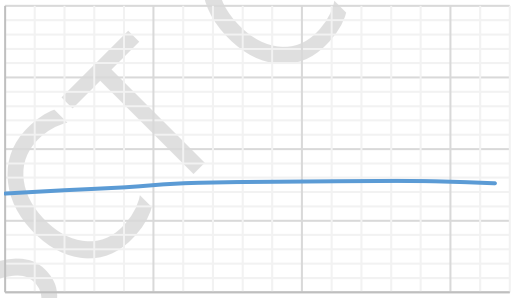

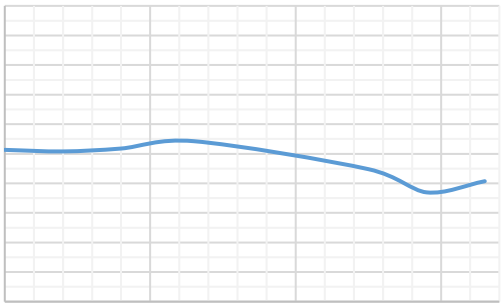

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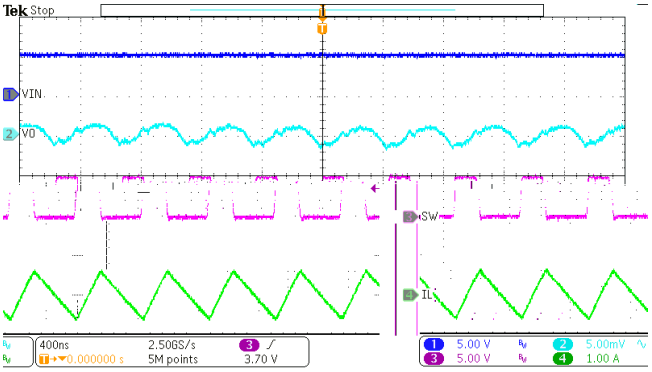
Tek Stop
50.0mV
1.00 A
-10.40000ms
5.00V
5.00V


Tek Stop
VIN
VO
SW
IL
400ns
2.50GS/s
5M points
3.70 V
5.00 V
5.00 V
5.00mV
1.00 A

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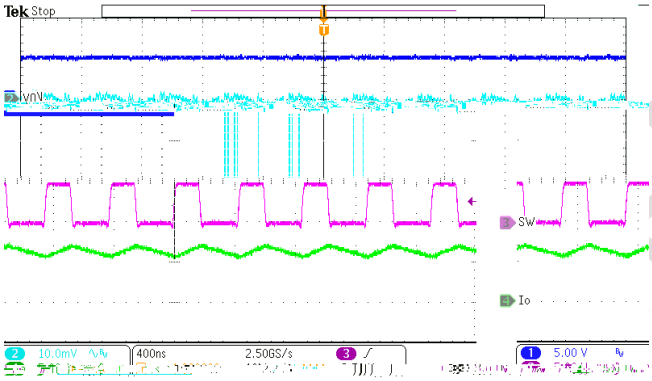
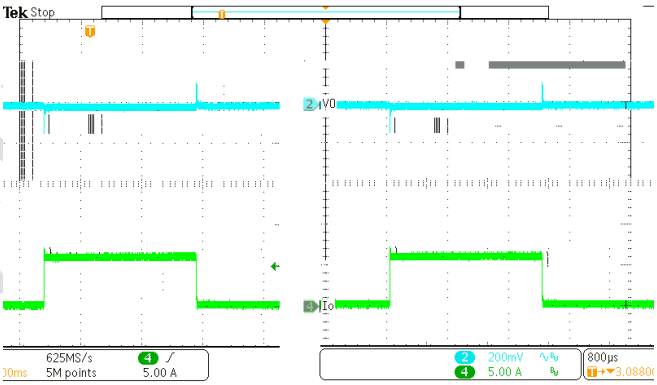
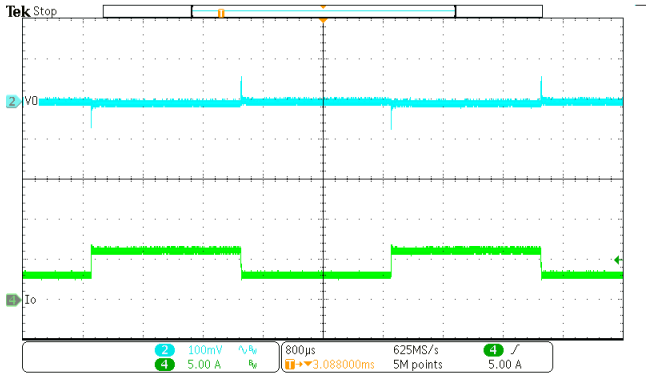
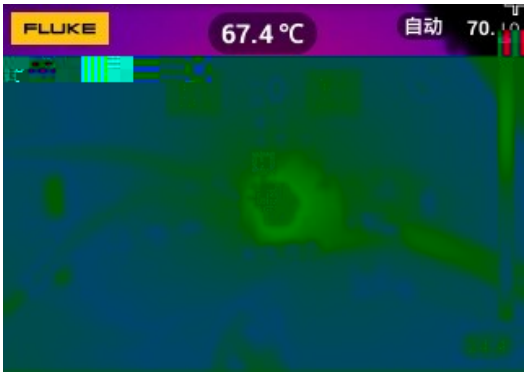
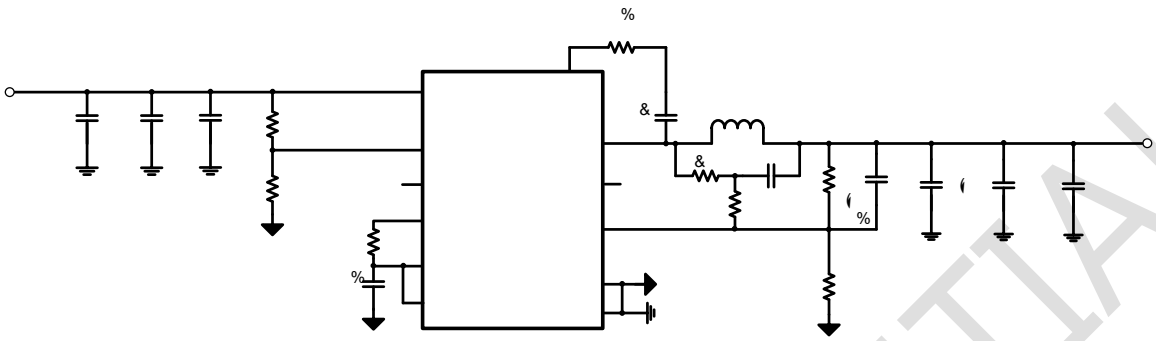

Tek Stop
VIN
SW
Io
10.0mV
400ns
2.50GS/s
5.00 V


Tek Stop
VO
Io
625MS/s
5M points
5.00 A
200mV
5.00 A
800µs


Tek Stop
VO
Io
100mV
5.00 A
800µs
625MS/s
5M points
5.00 A


FLUKE
67.4 °C
自动
70.



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The bottom layer is a large ground plane connected to the ground plane on top layer by vias it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss through the vias is of concern, plugging or tenting can be used to achieve a repeatable process.

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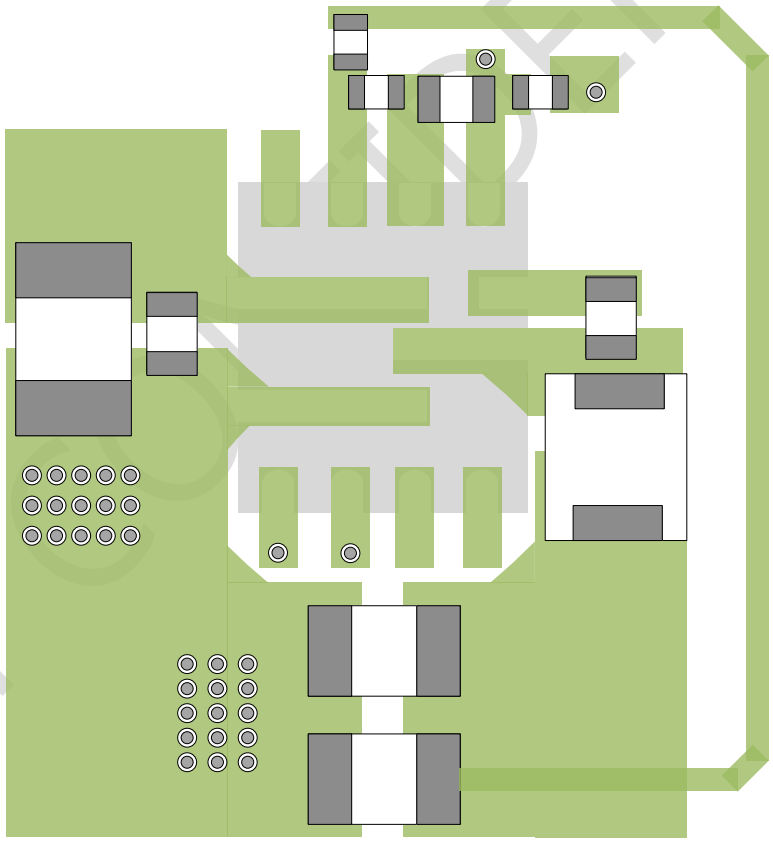

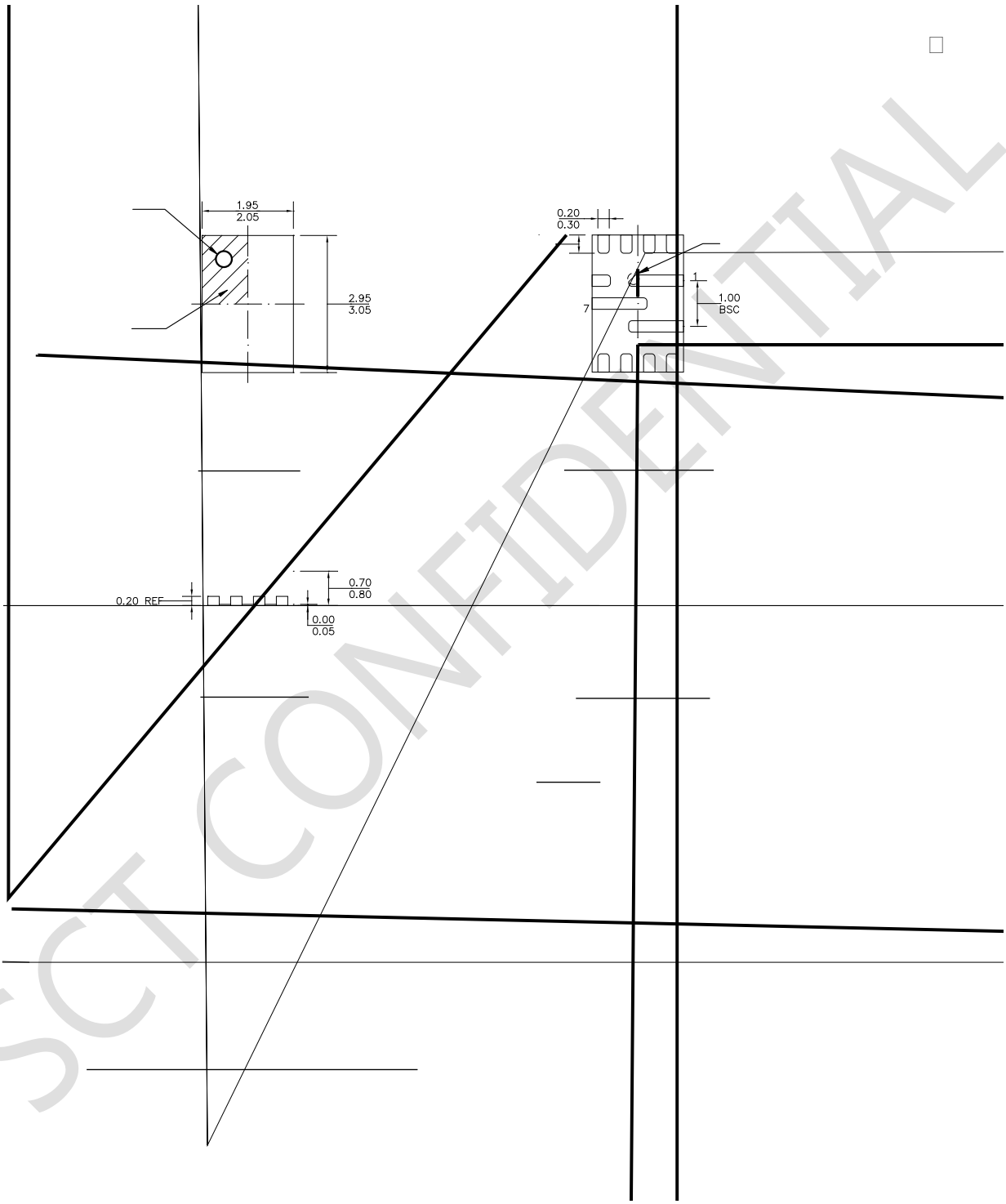

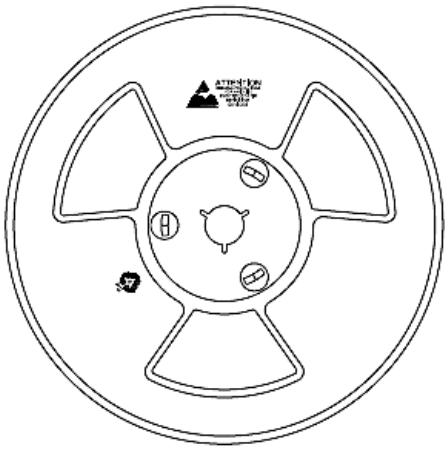

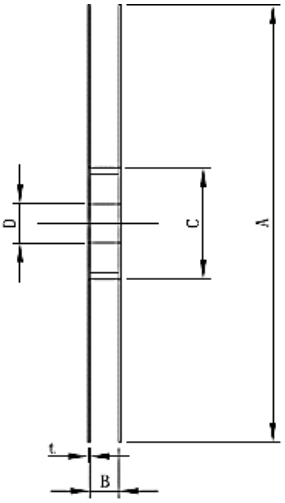
D
C
A
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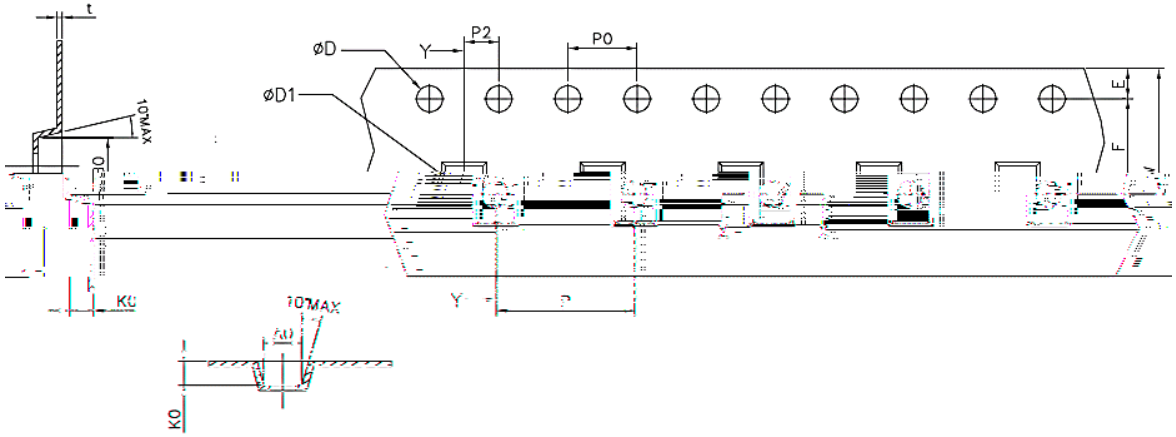
B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ØD
Y
P2
P0
ØD1
E
F
10MAX
K0
10MAX
K0

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