36V Vin Five Channels PMIC for Safety Applications

FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results:
  - Device Temperature Grade 1
- Wide Input Voltage Range: 3.5V-36V
- One Synchronous HV Buck Converter VOUT1:
  - Up to 3A Continuous Output Current
  - Output Voltage of 3.3/3.7/4.6/5V
- Dual Synchronous LV Buck Converters VOUT2, VOUT3:
  - Up to 2A Continuous Output Current
  - Output Voltage Range 0.8V to 2.35V with 50mV Steps
- One Synchronous LV Boost converter VOUT4:
  - Up to 500mA Continuous Output Current
  - Output Voltage of 5V
- One Low-Drop Regulator(LDO) VOUT5:
  - Up to 400mA Continuous Output Current
  - Output Voltage: 1.8/2.7/2.8/2.9/3.3V
- +/- 1.5% Feedback Reference Voltage
- Fixed 2.2MHz Switching Frequency with Integrated Frequency Dither for EMI Mitigation
- FCCM/PFM Selectable
- Programmable Power Sequencer for VOUT2, VOUT3, VOUT4 and VOUT5
- RESETB Output for System Management
- External Clock Synchronization
- Simple/QA Watchdog
- Integrated Protection Features:
  - Hiccup Over Current Protection
  - Output Over-voltage/Under-voltage Protection
  - Adjustable Input Voltage Under-voltage Lockout
  - Thermal Shutdown Protection
- Functional Safety Features:
  - Compliance with IOS26262 Development
  - Hardware Integrity up to Support ASIL-B System
  - ASIL-B Device Certification by TUV
  - BIST
- Up to 1MHz I2C Interface with Optional Packet Error-Checking (PEC)
- Available in QFN-24 (4mm*4mm)

DESCRIPTION

The SCT61451S device is a wide input power management IC with five channels output. The device is designed for MMICs in automotive and industrial radar applications.

The SCT61451S integrates one 3A HV Buck, two identical 2A LV Buck, one 500mA LV Boost and one 400mA LDO. Each channel output is continuously monitored, any over-voltage/under-voltage fault will be detected and the device will enter RESET state. All output voltages are pre-programmed, which saves external feedback divider and minimizes system solution. The switching frequency of HV Buck is 2.2MHz/400kHz selectable. The switching frequency is fixed 2.2MHz for LV buck and boost converters. The device features Frequency Spread Spectrum (FSS) with programmable jittering span of the switching frequency and modulation frequency to reduce the conducted EMI.

The device also integrates simple watchdog mode and QA watchdog mode. The dedicated WDI pin allows trigger pulse generated by MCU. Programmable watchdog window is suitable for a wide variety of applications. The RESETB output can be the sequencer of MCU to protect it from device fault.

The SCT61451S device has protection features such as thermal shutdown, short-circuit protection and over-voltage protection. Disabling all outputs via I2C can reduce the quiescent current to 0.85 mA.

The device has Built-in Self-Test (BIST) Diagnosis over internal analog and digital circuits. All critical comparator and data will be checked during power up stage.

The device is available in a QFN-24(4mm*4mm) Package.

APPLICATIONS

- ADAS
- 77GHz Radar
- Safety MCU

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ELECTRICAL CHARACTERISTICS

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DSON_H1}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		75	150	m Ÿ
R_{DSON_L1}	Low-side MOSFET on-resistance			50	120	m Ÿ
I_{LIM_HS1}	High-side power MOSFET current limit		4.2	5.2	6.2	A
I_{LIM_LSP1}	Low-side power MOSFET positive current limit		3.2	4.2	5.2	A
I_{LIM_LSN1}	Low-side power MOSFET negative current limit		0.8	2	3.2	A
R_{DIS1}	Discharge resistance	Output disabled		100	200	Ÿ
t_{ON_MIN1}						

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
R_{DIS3}	Discharge resistance	Output disabled		55	100	Ÿ
t_{ON_MIN3}	Minimum on-time			90		ns
$_{Phase3}$(1)	Switching phase			180		deg
VOUT4 (LV Boost)						
V_{S4}(1)	Supply voltage range		3		4.5	V
V_{ACC4}	Voltage accuracy	T_J = 25°C	-1		1	%
		T_J = -40°C~150°C	-1.5		1.5	%
R_{DSON_H4}	High-side MOSFET on-resistance			180	280	m Ÿ
R_{DSON_L4}	Low-side MOSFET on-resistance			60	100	m Ÿ
I_{LIM_LS4}	Low-side power MOSFET current limit		1.4	2	2.6	A
I_{LIM_HSP4}	High-side power MOSFET current limit		0.9	1.4	1.9	A
I_{LIM_HSN4}	High-side power MOSFET negative current limit		200	500	800	mA
R_{DIS4}	Discharge resistance	Output disabled		200	300	Ÿ
t_{ON_MIN4}	Minimum on-time			80		ns
$_{Phase4}$(1)	Switching phase			180		deg
VOUT5 (LDO)						
V_{ACC5}	Voltage accuracy	VOUT5 set to 2.8V	-1.5		1.5	%
V_{DROP_LDO}	LDO dropout voltage	VOUT1=3.3V, VOUT5=3.3V I_{OUT5}=400mA		120	300	mV
$L_{DO_LINE_REG}$	LDO line regulation	VOUT1=3.3V to 5V, VOUT5 set to 2.8V, I_{OUT5}=100mA		0.25		%/V
$L_{DO_LOAD_REG}$	LDO load regulation	VOUT1=3.3V, VOUT5 set to 2.8V, I_{OUT5}=10mA to 400mA		0.05		%
$I_{LIM_LDO_OCP}$	LDO over current limit	VOUT1=3.3V, VOUT5 set to 2.8V	480	600	720	mA
$I_{LIM_LDO_SCP}$	LDO output short current limit	VOUT1=3.3V, VOUT5=0V		140		mA
R_{DIS5}	Discharge resistance	Output disabled		100	200	Ÿ
Soft Start and Delay						
T_{SS}	Soft-start time	SS=0 to 1.1V		1		ms
T_{EN_ON}(1)	Device on time from EN high			2.8		ms
T_{ON_DELAY2}(1)	On delay for VOUT2		0		75	ms
T_{ON_DELAY3}(1)	On delay for VOUT3		0		75	ms
T_{ON_DELAY4}(1)	On delay for VOUT4		0		75	ms
T_{ON_DELAY5}(1)	On delay for VOUT5		0		75	ms

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ELECTRICAL CHARACTERISTICS (continued)

V_{IN}=12V, T_J=-40°C~150°C, typical values are tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
I2C Interface						
V_{IH}	High-level input voltage		1.2			V
V_{IL}	Low-level input voltage				0.4	V
V_{OL}	Low-level output voltage	I_{SINK}=4mA			0.4	V
F_{SCL}(1)	SCL clock frequency				1	MHz
T_{LOW}(1)	Low period of the SCL clock		500			ns
T_{HIGH}(1)	High period of the SCL clock		260			ns
T_{HD_STA}(1)	Hold time (repeated) START condition		260			ns
T_{SU_STA}(1)	Set-up time (repeated) START condition		260			ns
T_{HD_DAT}(1)	Data hold time		0			ns
T_{SU_DAT}(1)	Data set-up time		50			ns
T_R(1)	Rise time of both SCL and SDA signals				120	ns
T_F(1)	Fall time of both SCL and SDA signals				120	ns
T_{SU_STO}(1)	Set-up time for STOP condition		260			ns
C_B(1)	Capacitive load for each bus line				550	pF

(1) Guaranteed by sample and design characterization, not tested in production.

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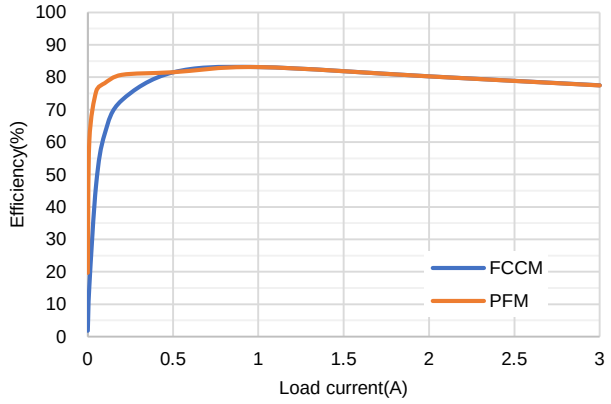
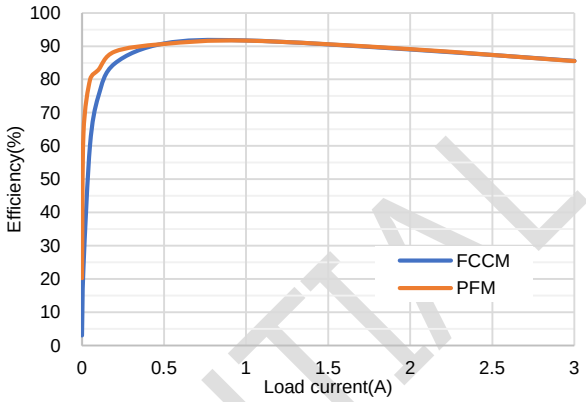
TYPICAL CHARACTERISTICS

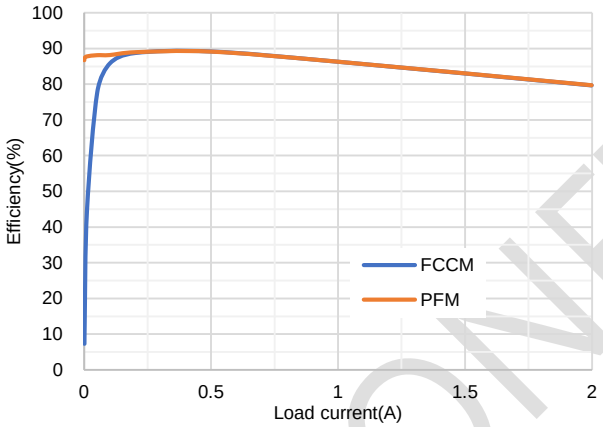
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



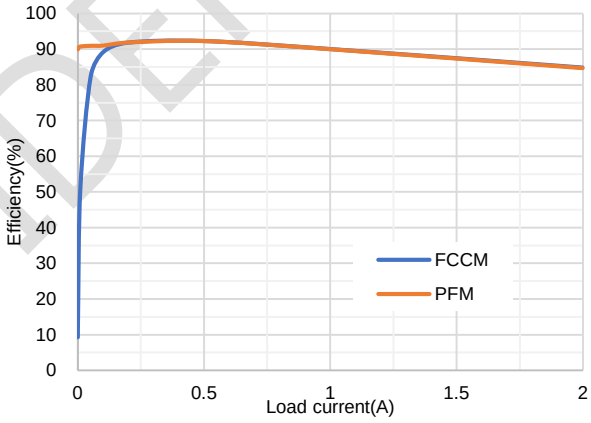
Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=2.2MHz



Buck1 Efficiency vs Load Current, V_{OUT1}=3.3V, f_{SW1}=400kHz



Buck2/3 Efficiency vs Load Current, $V_{OUT2/3}$=1.2V



Buck2 3 Efficiency vs Load Current, $V_{OUT2/3}$=1.8V

LDO PSRR, V_{OUT4}=2.8V, I_{OUT4}=10mA

LDO PSRR, V_{OUT4}=2.8V, I_{OUT4}=100mA

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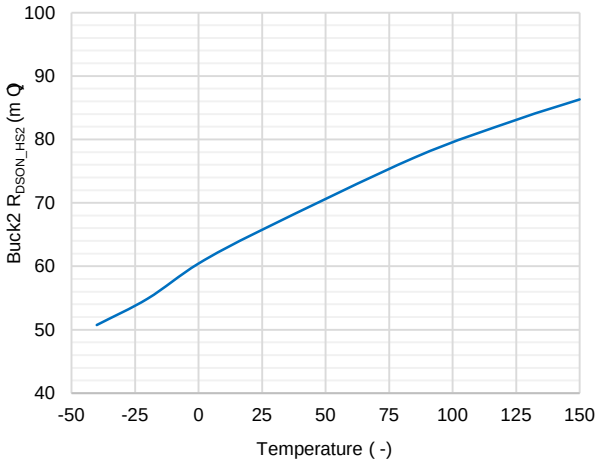
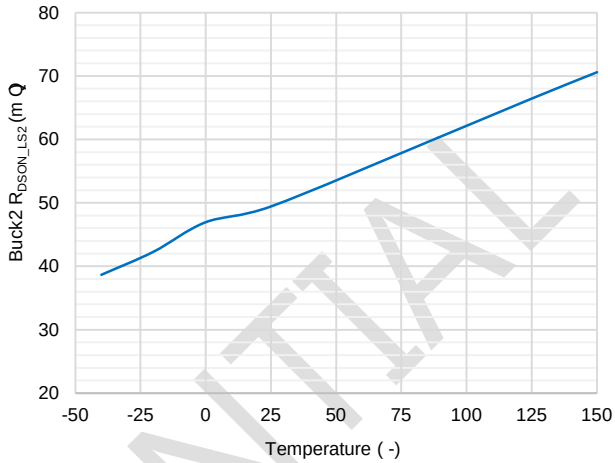
TYPICAL CHARACTERISTICS (continued)

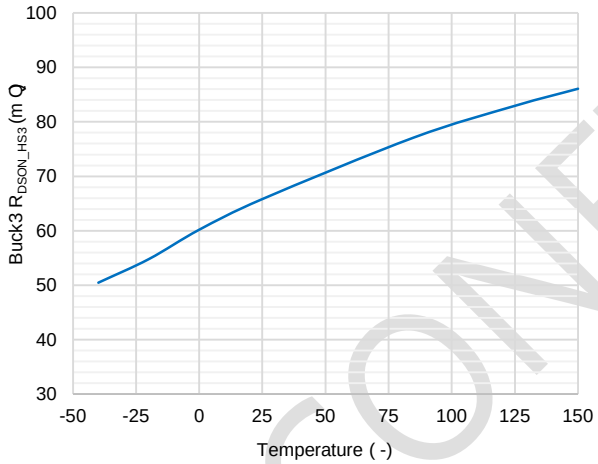
V_{IN}=12V, T_J=-40°C~125°C, unless otherwise noted.



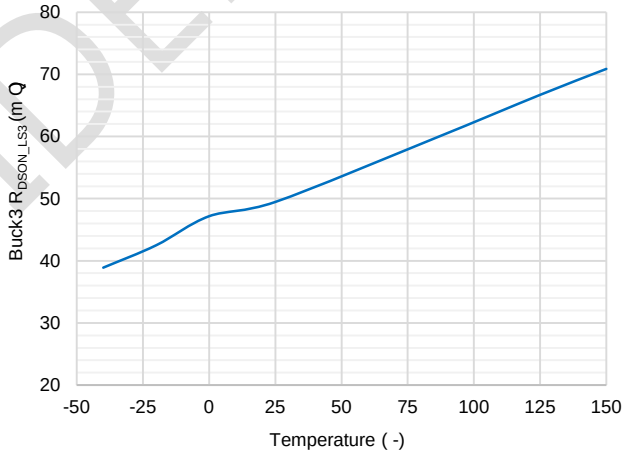
Buck2 R_{DSON_HS2} vs Temperature



Buck2 R_{DSON_LS2} vs Temperature



Buck3 R_{DSON_HS3} vs Temperature



Buck3 R_{DSON_LS3} vs Temperature

6 -04715.368

Boost R_{DSON_HS4} vs Temperature

Boost R_{DSON_LS4} vs Temperature

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FUNCTIONAL BLOCK DIAGRAM

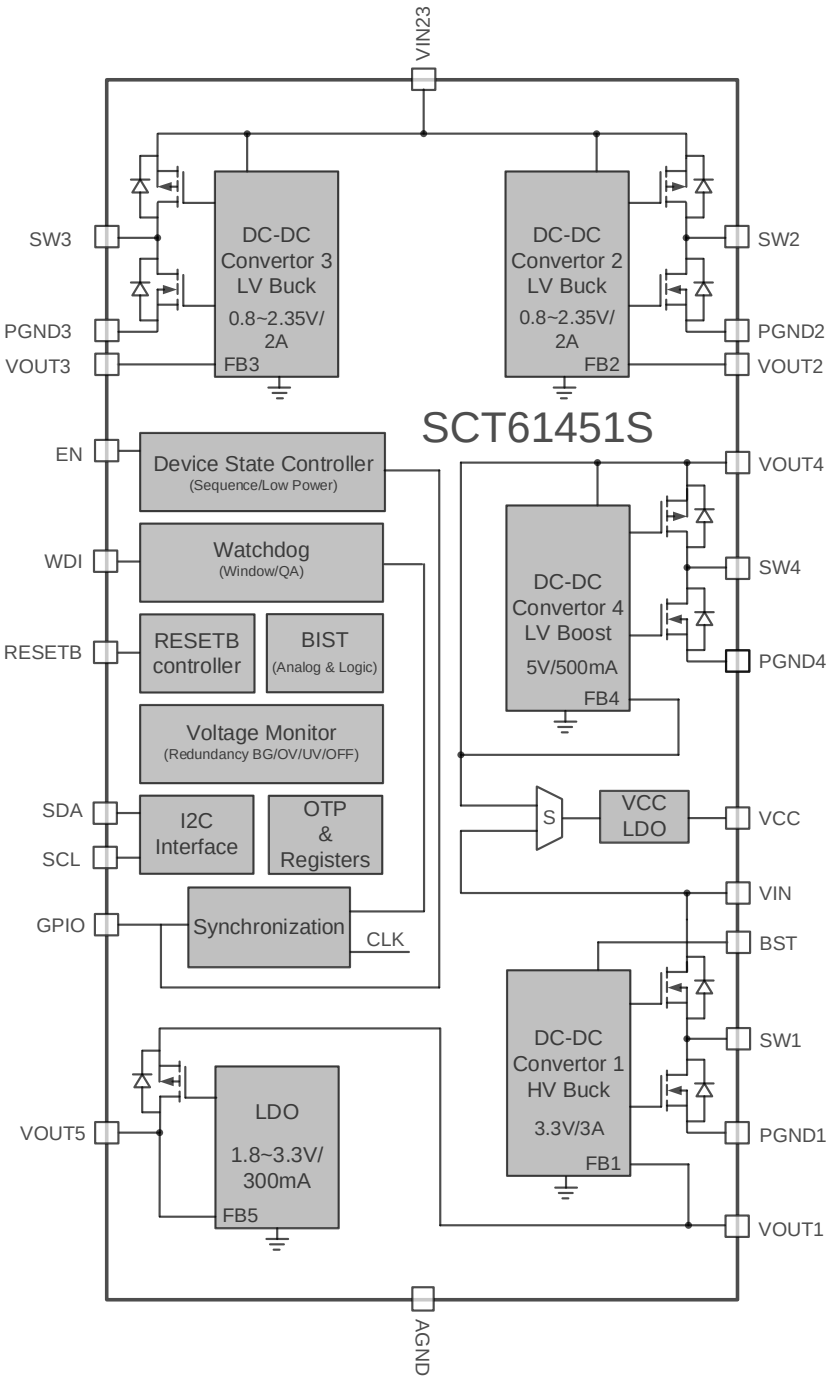

Figure 1. Functional Block Diagram

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Table 1. State and Function Matrix Table

State	Function											
	I2C	OTP load	Register reset	HV BUCK1	LV BUCK2	LV BUCK3	LV BOOST4	LDO5	Watchdog	OCP	DOVP/DUVP detect	TSD
IDLE	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LOADOTP	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LBIST	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DEEPSAFE	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
ABIST	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
POWERUP	ON	OFF	OFF	UP	UP	UP	UP	UP	OFF	ON	ON	ON
NORMAL	ON	OFF	OFF	ON	ON	ON	ON	ON	ON	ON	ON	

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- VIN/EN UVLO
- VCC OVP
- VIN OVP
- RESETB Stuck
- Loss of ground

ABIST State

To ensure safety mechanism work well, the device will check through all critical analog comparators before output start-up. If ABIST check is failed, the device will go back to DEEPSAFE state. ABIST will be implemented every time SCT61451S enter ABIST state, the device will transit to POWERUP state once ABIST is passed. Any ABIST failure will be recorded in register **SYS_STATE**.

POWERUP State

In POWERUP state, all rails will start-up following a dedicated sequence. Since the HV buck VOUT1 is the power supply for the other channels, VOUT1 is always set to start-up first. Then the other channels will rise after turn on delay time respectively. The turn on delay time for each is independent and can be adjusted via changing register **CONFIG_PU1** and **CONFIG_PU2**, thus flexible sequence is available. Deep OV/UV protection is activated to protect channels from destructive OV/UV risk. If all channels finish soft-start and they are within power good range, the RESETB rising timer begins. Once the timer is expired, the device will enter NORMAL state and RESETB will output high. If deep safe event occurs, the state will transit to DEEPSAFE state directly.

NORMAL State

The NORMAL state is the normal running of device with all outputs on. The RESETB pin is released after specific delay time upon entering this state. If watchdog is enabled by register **CONFIG_WD3**, watchdog window will start after setting delay time. The delay time is configured by **WD_1UD[2:0]** in register **CONFIG_WD3**. MCU should feed the watchdog via WDI pin or write answer to specified register periodically. When operating in NOMRAL state, the device will go to RESET state once reset event occurs.

RESET State

All outputs keep on in this state, the device will transit from NORMAL state to RESET state when any of below reset event occurs:

- VOUT1's output is out of OV/UV protection range
- VOUT2's output is out of OV/UV protection range
- VOUT3's output is out of OV/UV protection range
- VOUT4's output is out of OV/UV protection range
- VOUT5's output is out of OV/UV protection range
- Watchdog Failure

When the device enters RESET state, the RESETB pin will assert for a holding time. The device will go back to NORMAL state automatically once the holding time is expired and no reset event, which can be configured in register **CONFIG_T1** via I2C. Upon entering NOMRAL state Watchdog failure counter will be reset and start running again. Then MCU should feed the watchdog again.

VIN and EN UVLO

When the VIN pin voltage rises above 3.2V and the EN pin voltage exceeds the enable threshold of 1.2V, the device is enabled. And the device disables when the VIN pin voltage falls below 2.8V or when the EN pin voltage is below 1.0V.

EN pin is connected internally to ground allows the device to be disabled when EN pin is floating to simplify the system design.

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High Efficiency Regulators

The switching frequency of HV Buck is 2.2MHz/400kHz selectable. All the LV bucks and boost employ 2.2MHz fixed frequency peak current mode control. Forced continuous conduction mode (FCCM) allows the device to have a high output performance when light load. Built-in UVLO ensures all channels are capable of regulated output under the operating VIN range. Soft-start is fixed at 1ms for all channels. VOUT1 will always be the firstly built rail after power on, the other rails can be configured with range 0ms to 75ms turn on delay. Then the device can achieve a variety of sequence to fit power system.

The VOUT1 is a HV synchronous buck converter directly power from VIN pin. It's regulated at 3.3V with up to 3A continuous current. An external 100nF ceramic bootstrap capacitor between BST and SW1 pin powers high-side power MOSFET gate driver. The bootstrap capacitor voltage is charged from an integrated voltage regulator when high-side power MOSFET is off and low-side power MOSFET is on. Note VOUT1 is the power supply for VOUT2/3/4/5.

The VOUT2 and VOUT3 are two identical LV synchronous buck converter power by VOUT1. Their output can be configured via I2C range from 0.8V to 2.35V with 50mV step. Each is capable of 2A continuous current. To further improve the EMI performance, the VOUT2 and VOUT3 will operate with 180 phase-shifted clock.

The VOUT4 is a LV synchronous boost converter also power by VOUT1. It's regulated at 5V with up to 500mA continuous current.

The VOUT5 is a low-drop regulator(LDO) also powered by VOUT1. The LDO output is factory-programmed at 1.8V, 2.7V, 2.8V, 2.9V or 3.3V with up to 400mA continuous output current.

The converters have proprietary designed gate driver scheme to resist switching node ringing without sacrificing MOSFET turn-on and turn-off time, which further erases high frequency radiation EMI noise caused by the MOSFETs hard switching.

Each output voltage is continuously monitored during operation, the OV/UV threshold can be adjusted independently in register **CONFIG_PGSEL1** and **CONFIG_PGSEL2**.

Deep Over Voltage Protection

If any output exceeds the deep over voltage protection threshold 115%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_OVP_SEL[1:0]**.

Deep Under Voltage Protection

If an output falls below the deep under voltage protection threshold 75%, all outputs will shut off for the hiccup time. When hiccup ends, the normal power up sequence will start again following turn on delay setting in register. When entry hiccup, the output discharge will operate during the hiccup time. The threshold can be configured by bits **DEEP_UVP_SEL[1:0]**.

Thermal Shutdown

The thermal shutdown protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 175°C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 155°C, the device will restart with internal soft start phase.

Over Current Protection (OCP)

The converters implement over current protection with cycle-by-cycle limiting high-side MOSFET peak current and also low-side MOSFET valley current to avoid inductor current running away during unexpected overload and hiccup protection in output hard short condition. When overload or hard short happens, the converter cannot provide output current to satisfy loading requirement even though the inductor current has already been clamped at over current limitation. Thus, output voltage drops below regulated voltage continuously. When peak current point is kicked for continuous 32 times, the converter stops switching, the device will jump to DEEPSAFE state. The hiccup protection mode greatly reduces the average short circuit current to alleviate thermal issues and protect the regulator.

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For the boost, the device provides a load disconnect function, which completely disconnects the output from the input during overload. Then output short to ground fault is protected.

Frequency Spread Spectrum

To meet CISPR and automotive EMI compliances, the SCT61451S implements Frequency Spread Spectrum (FSS) function. The FSS circuitry shifts the 2.2MHz switching frequency within ±3%/±6%/±9%/±4.5% range and 4.5k/9kHz period triangular or pseudo modulation. Therefore, the SCT61451S can guarantee that the switching frequency does not drop into the 1.8MHz AM band limit.

Frequency Foldback

To avoid meeting minimum on time, the HV buck VOUT1 will reduce switching frequency actively when input voltage rising high. Other channel's frequency is unchanged.

When VIN greatly drops and minimum off time of HV buck VOUT1 is kicked, the VOUT1 enter dropout mode and also reduce its frequency to get max output.

RESETB Indicator

The RESETB indicator will assert when reset event occurs. It will reset MCU if it fails to feed watchdog, MCU then can reloading program to ensure the program run well. The RESETB pin is an open-drain output and can be connected to various I/O level through pull-up resistor. The reset event mapping to

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polynomial: x8 + x6 + x5 + x4 + 1. Any violation except **WD_LFSR[0]** violation will make the WD error counter plus one. When WD error counter reaches the **WD_FAIL_CNT[0]** (1 or 2 times), a WD Failure is reported and device enters RESET state.

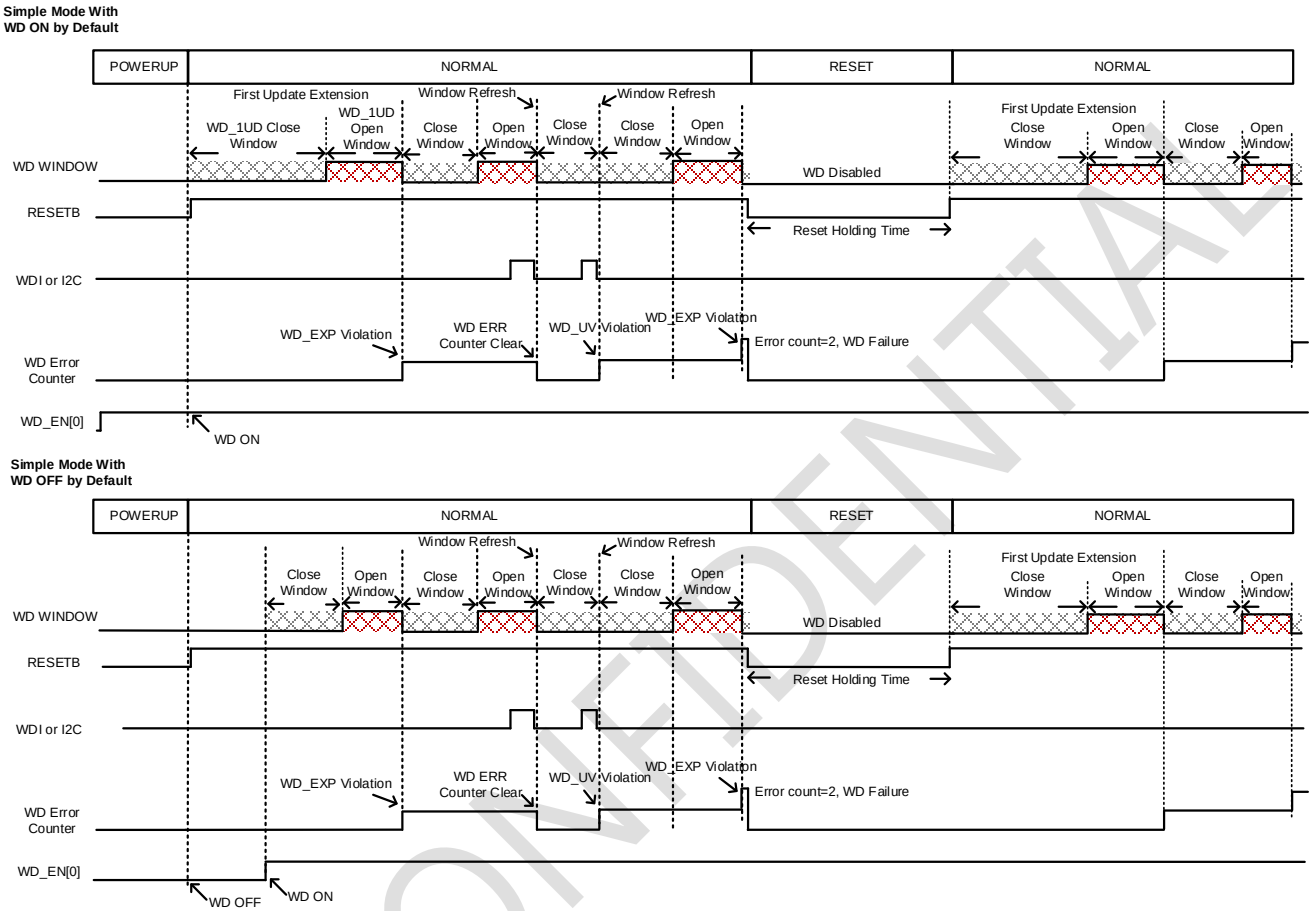

Figure 3a. Simple Watchdog Error Timing

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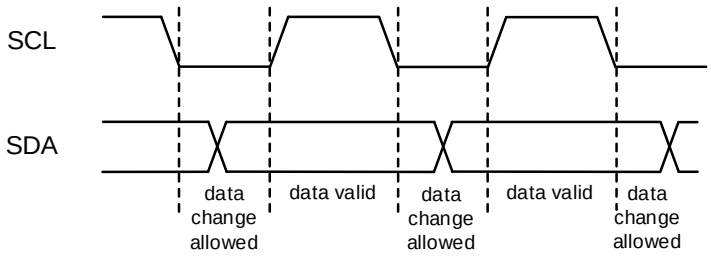

Figure 4. Data Validity Diagram

START and STOP Conditions

The data transfer always generates START and STOP conditions to announce the process. A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. Both the START and STOP conditions are generated by master on bus.

The bus is considered to be busy after START condition and released after STOP condition. A repeated START condition during transmission is also valid and will be regard as a new START condition.

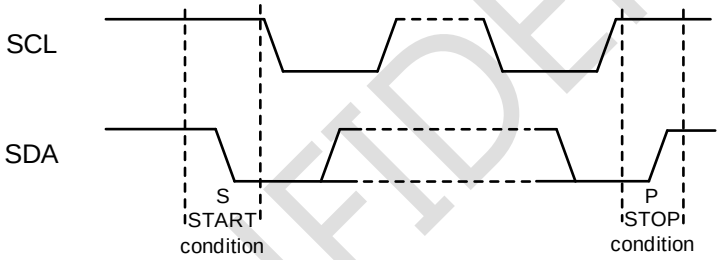

Figure 5. START and STOP Conditions Diagram

Data Transmission

The transferred byte consists of eight bits with the Most Significant Bit (MSB) first. After each byte is transferred, the master will release the SDA line and generate the ninth acknowledge clock pulse on SCL line. The SCT61451S will pull the SDA line LOW during this acknowledge clock, to announce a successful reception and next byte may be sent. If the master is receiver and the last byte is received, it still generates the ninth acknowledge clock pulse but SDA line will not be pulled LOW. It's called not acknowledge signal and indicates the end of transmission.

After the START condition, the master must send a slave address as the first addressing byte. The slave address is seven bits long followed by an eighth R/W bit. The R/W bit defines the data direction. Set the R/W bit to 0 to indicate write command, and a 1 indicates read command. The slave address is factory-programmed between 0x38 through 0x3B, see DEVICE ORDER INFORMATION for details.

Packet Error Checking (PEC)

The SCT61451S supports optional packet error checking (PEC) byte during the I2C communication. PEC can significantly increase fault coverage on the I2C interface. The PEC byte is implemented through CRC-8 polynomial of x8 + x2 + x +1. The PEC byte does not take ACK, NACK, START, STOP, Repeated START bits into calculation. The PEC byte is calculated on the register address and data byte over the entire message from the first START condition, note that the slave address is removed both in write and read command. When PEC is enabled, the device will reject the write command if the master send an incorrect PEC byte. When in read mode with PEC enabled, the master should acknowledge the data byte thus then the device will send the PEC byte. The PEC can be configured by **PEC_EN** in register **CONFIG_FSS**.

Write Data Format

A write to the device includes transmission of the following:

- START condition
- Slave address with the write bit set to 0

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- z 1 byte of data to register address
- z 1 byte of data to the command register
- z STOP condition

Read Data Format

A read from the device includes the following:

- z Transmission of a START condition
- z Slave address with the write bit set to 0
- z 1 byte of data to register address
- z Restart condition
- z Slave address with read bit set to 1
- z 1 byte of data to the command register
- z STOP condition

Figure 6 illustrates the proper format for one frame.

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APPLICATION INFORMATION

Typical Application

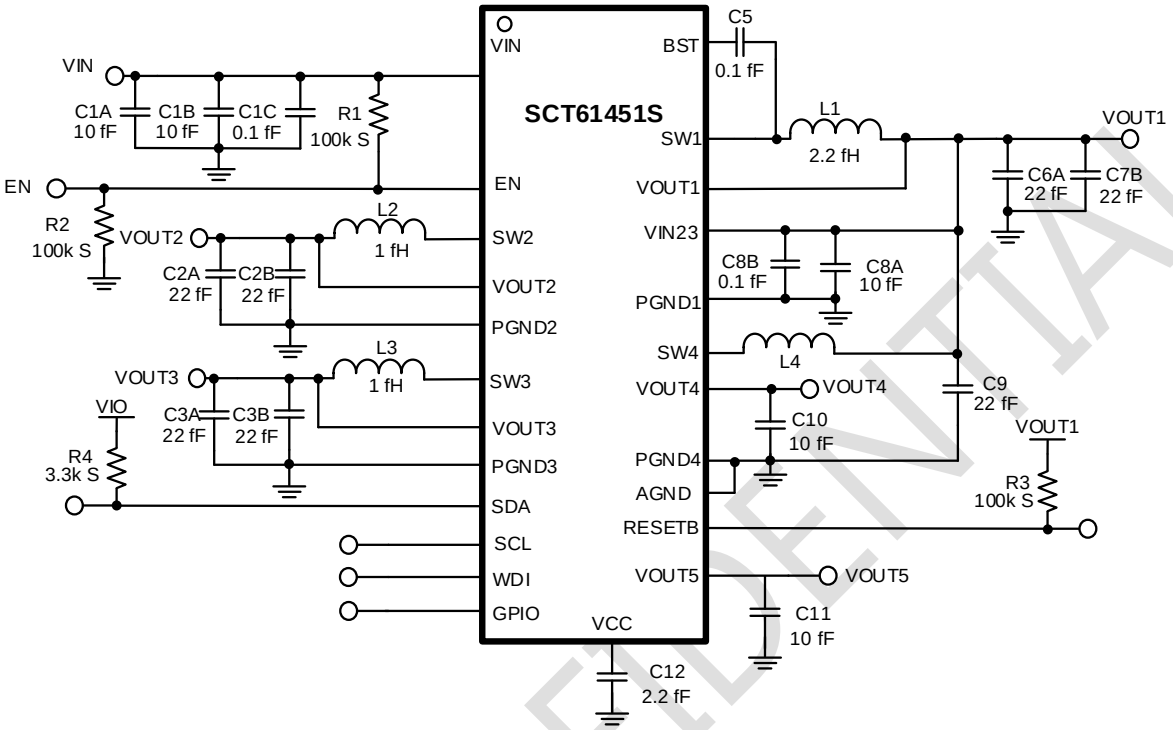

Figure 8. Application Schematic, 3.5V to 36V, PMIC Regulator at 2.2MHz

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal 3.5V to 36V
Output Voltage	VOUT1: 3.3V VOUT2: 1.2V VOUT3: 1.8V VOUT4: 5V VOUT5: 2.8V
Maximum Output Current	VOUT1: 3A (in total) VOUT2: 2A VOUT3: 2A VOUT4: 500mA VOUT5: 400mA
Switching Frequency	2.2MHz
Output Voltage Ripple (peak to peak)	VOUT1: 10mV VOUT2: 5mV VOUT3: 5mV VOUT4: 20mV

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Under Voltage Lock-Out

An external voltage divider network of R_1 from the input to EN pin and R_2 from EN pin to the ground can set a higher input voltage's Under Voltage Lock-Out (UVLO) threshold. The UVLO has two thresholds, one for power up when the input voltage is rising and the other for power down or brown outs when the input voltage is falling. Use Equation 1 and Equation 2 to calculate the values of R_1 and R_2 resistors.

$$8_{\text{á Ü æ ø}} = 1 + \frac{4_5}{4_6} \text{ p } Û8_{¾ \text{ ç å Ü æ ø}} \quad (1)$$

$$8_{Ù Ô ß ß} = 1 + \frac{4_5}{4_6} \text{ p } Û8_{¾ Ç Ù Ô ß ß} \quad (2)$$

where

- V_{rise} is rising threshold of Vin UVLO
- V_{fall} is falling threshold of Vin UVLO
- V_{ENrise} is rising threshold of EN UVLO
- V_{ENfall} is falling threshold of EN UVLO

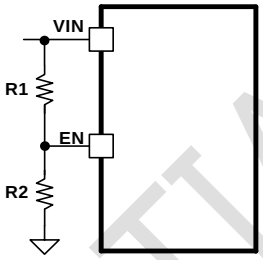

Figure 9. System UVLO by enable divide

Inductor Selection

There are several factors should be considered in selecting inductor such as inductance, saturation current, the RMS current and DC resistance(DCR). Larger inductance results in less inductor current ripple and therefore leads to lower output voltage ripple. However, the larger value inductor always correspon

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- LIR is coefficient of I_{LPP} to I_{OUT}

The total current flowing through the inductor is the inductor ripple current plus the output current. When selecting an inductor, choose its rated current especially the saturation current larger than its peak operation current and RMS current also not be exceeded. Therefore, the peak switching current of inductor, I_{LPEAK} and I_{LRMS} can be calculated as in equation 5 and equation 6.

$$I_{LPEAK} = I_{OUT} + \frac{I_{LPP}}{2} \quad (5)$$

$$I_{LRMS} = \sqrt{(I_{OUT})^2 + \frac{5}{56} \times (I_{LPP})^2} \quad (6)$$

Where

- I_{LPEAK} is the inductor peak current
- I_{OUT} is the DC load current
- I_{LPP} is the inductor peak-to-peak current
- I_{LRMS} is the inductor RMS current

For a boot converter, the peak-to-peak ripple current in the inductor I_{LPP} can be calculated as

$$I_{LPP_BOOST} = \frac{1}{L \times \left(\frac{5}{f_{SW} \times V_{OUT}} + \frac{5}{V_{IN}}\right) \times 0.9} \quad (7)$$

Where

- I_{LPP_BOOST} is the inductor peak-to-peak current of boost
- L is the inductance of inductor
- f_{SW} is the switching frequency
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Calculate the inductor DC current as in equation 8

$$I_{DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \quad (8)$$

Therefore, the peak switching current of inductor, I_{LPEAK}, is calculated as

$$I_{LPEAK} = I_{DC} + \frac{I_{LPP}}{2} \quad (9)$$

In overloading or load transient conditions, the inductor peak current can increase up to the switch current limit of the device. The most conservative approach is to choose an inductor with a saturation current rating greater than peak current limit. Because of the maximum I_{LPEAK} limited by device, the maximum output current that the device can deliver also depends on the inductor current ripple. Thus, the maximum desired output current also affects the selection of inductance. The smaller inductor results in larger inductor current ripple leading to a lower maximum output current.

Input Capacitor Selection

The input current to the step-down DCDC converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down DCDC converter while maintaining the DC input voltage. Use capacitors with low ESR for better performance. Ceramic capacitors with X5R or X7R dielectrics are usually suggested because of their low ESR and small temperature coefficients, and it is strongly recommended to use another lower value capacitor (e.g. 0.1uF) with small package size (0603) to filter high frequency switching noise. Place the small size capacitor as close to VIN and GND pins as possible.

For buck converter, the voltage rating of the input capacitor must be greater than the maximum input voltage. And the capacitor must also have a ripple current rating greater than the maximum input current ripple. The RMS current in the input capacitor can be calculated using Equation10.

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$$I_{CIN_RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (10)$$

The worst case condition occurs at $V_{IN}=2*V_{OUT}$, where:

$$I_{CIN_RMS} = 0.5 \times I_{OUT} \quad (11)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

When selecting ceramic capacitors, it needs to consider the effective value of a capacitor decreasing as the DC bias voltage across a capacitor increasing.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 12 and the maximum input voltage ripple occurs at 50% duty cycle.

$$\Delta V_{IN} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (12)$$

For the boost converter power stage, because of the inductor current ripple, the input voltage changes if there is parasitic inductance and resistance between the power supply and the inductor. It is recommended to have enough input capacitance to make the input voltage ripple less than 100mV. Generally, a 10) input capacitance is recommended for most applications. Choose the right capacitor value carefully by considering high-capacitance ceramic capacitors DC bias effect, which has a strong influence on the final effective capacitance.

Bootstrap Capacitor Selection

$) F H U D P L F F D S D F L W R U is connected between the BST pin and SW1 pin for proper operation. A ceramic capacitor with X5R or better grade dielectric is recommended. The capacitor should have a 10V or higher voltage rating.

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

For buck converter, the output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 13 desired.

$$\Delta V_{OUT_BUCK} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{8 \times L \times f_{SW}^2 \times V_{IN} \times C_{OUT}} \quad (13)$$

Where

- ΔV_{OUT_BUCK} is the output voltage ripple of buck converter
- f_{SW} is the switching frequency
- L is the inductance of inductor
- C_{OUT} is the output capacitance
- V_{OUT} is the output voltage
- V_{IN} is the input voltage

Due to capacitor’s degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their capacitance at rated voltage. Therefore, leave margin on the voltage rating to ensure adequate effective capacitance. Typically, two 10) F H U D P L F R X W S X W F D S D F L W R U V Z R U N I

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For boost converter, typically, a 22) F H U D P L F R X W S X W F D S D F L W R U V Z R U N I R U P R V W D S S can be used to improve the load transient response. From the required output voltage ripple, use the below equation to calculate the minimum required effective capacitance

$$C_{OUT_MIN} = \frac{(V_{OUT} - V_{IN_MIN}) \times I_{OUT}}{V_{OUT} \times \Delta V_{OUT_BOOST} \times f_{SW}} \quad (14)$$

where

- ΔV_{OUT_BOOST} is output voltage ripple caused by charging and discharging of the output capacitor of boost
- V_{IN_MIN} is the minimum input voltage of boost converter.
- V_{OUT} is the output voltage.
- I_{OUT} is the output current.
- f_{SW} is the converter switching frequency.

Table 3. Recommended BOM for Typical Application

Output Rail	Frequency (MHz)	L (uH)	Input Capacitor (uF)	Output Capacitor (uF)
Buck1	2.2	2.2	2 x 10+1 x 0.1	2 x 22
Buck2	2.2	1	10+1 x 0.1	2 x 10
Buck3	2.2	1		2 x 10
Boost4	2.2	1	22	10
LDO5	-	-	-	10
VCC	-	-	-	2.2

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Application Waveforms

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.1V, V_{OUT3}=1.5V, V_{OUT4}=5V, V_{OUT5}=2.8V, unless otherwise noted

Figure 10. Power On (Io2=Io3=2A, Io4=0.5A)

Figure 11. Power Off (Io2=Io3=2A, Io4=0.5A)

Figure 12. EN On (Io2=O

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Application Waveforms (continued)

Vin=12V, V_{OUT1}=3.3V, V_{OUT2}=1.1V, V_{OUT3}=1.5V, V_{OUT4}=5V, V_{OUT5}=2.8V, unless otherwise noted

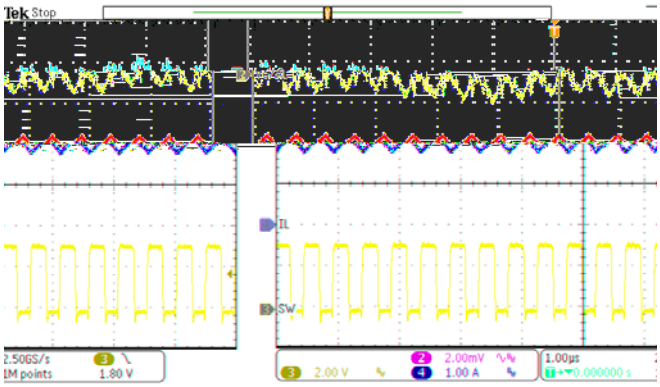

Figure 16. Buck3 Steady State (Io3 = 2A)

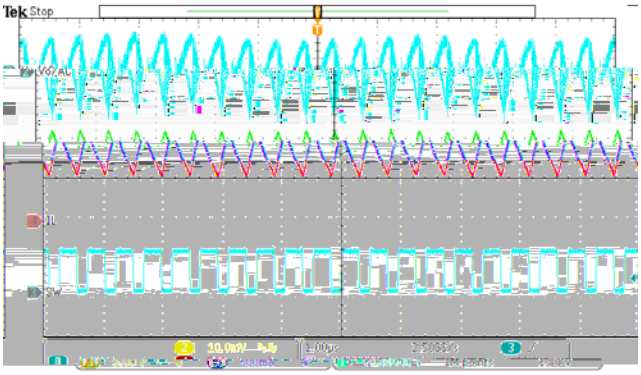

Figure 17. Boost4 Steady State (Io4 = 500mA)

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Layout Guideline

Proper PCB layout is a critical for device's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The

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				10: Scale=2.5ms. Delay ranges from 0-37.5ms 11: Scale =5ms. Delay ranges from 0-75ms

CONFIG_T2 [7:0]				
ADDRESS: 0x03				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	DF_SCALE	W/R	OV/UV Digital Filter. Adds additional filtering to all OV/UV comparators.	Analog Filter Time = 10µs. Added Digital Filter Timeo! =DF[5:0] x 2µs, when DF_SCALE=0, =DF[5:0] x 10µs, when DF_SCALE=1.
[4:0]	DF	W/R		

CONFIG_EN [7:0]				
ADDRESS: 0x05				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**

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ON_DELAY4[3:0] x 2.5ms
when DELAY_SCALE=11, t_{ON_DELAY4} = ON_DELAY4[3:0] x 5ms

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				1 = WD ERROR is mapped to RESETB pin

STATUV [7:0]				
ADDRESS: 0x0A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	UV	Read Clear	UV Comparator Status for all channels with Digital Filter.	0 = All enabled channels are above UV threshold after DF 1 = Any enabled channel is below UV threshold after DF
[6]	RESERVED	R	/	/
[5]	UV_WAR5	Read Clear	UV warning for OUT5, Digital Filter is not included	0 = OUT5 is above UV threshold before DF 1 = OUT5 is below UV threshold before DF
[4]	UV_WAR4	Read Clear	UV warning for OUT4, Digital Filter is not included	0 = OUT4 is above UV threshold before DF 1 = OUT4 is below UV threshold before DF
[3]	UV_WAR3	Read Clear	UV warning for OUT3, Digital Filter is not included	0 = OUT3 is above UV threshold before DF 1 = OUT3 is below UV threshold before DF
[2]	UV_WAR2	Read Clear	UV warning for OUT2, Digital Filter is not included	0 = OUT2 is above UV threshold before DF 1 = OUT2 is below UV threshold before DF
[1]	UV_WAR1	Read Clear	UV warning for OUT1, Digital Filter is not included	0 = OUT1 is above UV threshold before DF 1 = OUT1 is below UV threshold before DF
[0]	RESERVED	R	/	/

STATOV [7:0]				
ADDRESS: 0x0B				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	OV	Read Clear	OV Comparator Status for all channels with Digital Filter.	0 = All enabled channels are below OV threshold after DF 1 = Any enabled channel is above OV threshold after DF
[6]	RESERVED	R	/	/
[5]	OV_WAR5	Read Clear	OV warning for OUT5, Digital Filter is not included	0 = OUT5 is below OV threshold before DF 1 = OUT5 is above OV threshold before DF
[4]	OV_WAR4	Read Clear	OV warning for OUT4, Digital Filter is not included	0 = OUT4 is below OV threshold before DF 1 = OUT4 is above OV threshold before DF
[3]	OV_WAR3	Read Clear	OV warning for OUT3, Digital Filter is not included	0 = OUT3 is below OV threshold before DF

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				1 = OUT3 is above OV threshold before DF
[2]	OV_WAR2	Read Clear	OV warning for OUT2, Digital Filter is not included	0 = OUT2 is below OV threshold before DF 1 = OUT2 is above OV threshold before DF
[1]	OV_WAR1	Read Clear	OV warning for OUT1, Digital Filter is not included	0 = OUT1 is below OV threshold before DF 1 = OUT1 is above OV threshold before DF
[0]	RESERVED	R	/	/

STATOFF [7:0]				
ADDRESS: 0x0C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	RESERVED	R	/	/
[5]	OFF5	Read Clear	OFF Comparator Status for OUT5	0 = OUT5 is above OFF threshold 1 = OUT5 is below OFF threshold
[4]	OFF4	Read Clear	OFF Comparator Status for OUT4	0 = OUT4 is above OFF threshold 1 = OUT4 is below OFF threshold
[3]	OFF3	Read Clear	OFF Comparator Status for OUT3	0 = OUT3 is above OFF threshold 1 = OUT3 is below OFF threshold
[2]	OFF2	Read Clear	OFF Comparator Status for OUT2	0 = OUT2 is above OFF threshold 1 = OUT2 is below OFF threshold
[1]	OFF1	Read Clear	OFF Comparator Status for OUT1	0 = OUT1 is above OFF threshold 1 = OUT1 is below OFF threshold
[0]	RESERVED	R	/	/

STATD [7:0]				
ADDRESS: 0x0D				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	RESERVED	R	/	/
[6]	CLK_ERR	Read Clear	CLK fault indicator	0 = No fault detected 1 = CLK error detected
[5]	SUP_ERR	Read Clear	Supply fault indicator, include VCC OV fault and VIN OV fault	0 = No fault detected 1 = VCC OV or VIN OV detected
[4]	RST_ENTER	Read Clear	RESET state indicator	0 = No fault detected 1 = RESET state has entered since the last read.
[3]	DEEPSAFE_ENTER	Read Clear	DEEPSAFE state indicator	0 = No fault detected 1 = DEEPSAFE state has entered since the last read.
[2]	PIN_ERR	Read Clear	Pin fault indicator, include RESETB Pin stuck fault and GND pin LOSS fault	0 = No fault detected 1 = RESETB Short to supply detected or pull-down fail or GND LOSS since the last read
[1]	THSD	Read Clear	Thermal Shutdown Indication	0 = No thermal shutdown 1 = Thermal shutdown has occurred since last read

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				11 = Reserved
[5]	RESERVED	R	/	/
[4]	VIN_OVP_EN	W/R	Enable of VIN OVP. When VIN>43V, part enter DEEPSAFE mode.	0 = Disabled 1 = Enabled
[3:2]	VIN_START	W/R	VIN start threshold at VIN rising	00 = 3.2V; 01 = 4V; 10 = 5V; 11 = 6V
[1:0]	VIN_STOP	W/R	VIN stop threshold at VIN falling	00 = 2.8V; 01 = 3.5V; 10 = 4.5V; 11 = 5.5V

CONFIG_PFM [7:0]				
ADDRESS: 0x12				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:4]	RESERVED	R	/	/
[3]	PFM4	W/R	BOOST4 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[2]	PFM3	W/R	BUCK3 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[1]	PFM2	W/R	BUCK2 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM
[0]	PFM1	W/R	BUCK1 FCCM/PFM mode selection when NORMAL mode.	0 = FCCM 1 = PFM

CONFIG_WD1 [7:0]				
ADDRESS: 0x13				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7]	WD_MODE	W/R	Simple Windowed Watchdog Enable	0 = QA watchdog enabled 1 = Simple watchdog enabled
[6]	WD_SCALE	W/R	Watchdog Clock Divider Scale	0 = 128us 1 = 128us*64
[5:0]	WD_CLK	W/R	Watchdog Clock Divider	tWDCLK = (

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[4]	WD_FAIL_CNT	W/R	Watchdog Failure counter config. When Watchdog failure times reach the counter, report to RESETB and status register.

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[3:2]	RESERVED	R	/	/
[1:0]	PG5_SEL	W/R	OUT5 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%

CONFIG_PGSEL2 [7:0]				
ADDRESS: 0x1A				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:6]	PG4_SEL	W/R	OUT4 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%
[5:4]	PG3_SEL	W/R	OUT3 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%
[3:2]	PG2_SEL	W/R	OUT2 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%
[1:0]	PG1_SEL	W/R	OUT1 OV/UV threshold selection.	00 = Reserved; 01 = ±6%; 10 = ±8%; 11 = ±10%

I2C_LOCK [7:0]				
ADDRESS: 0x1C				
BITS	**FIELD**	**TYPE**	**DESCRIPTION**	**DECODE**
[7:1]	RESERVED	R	/	/

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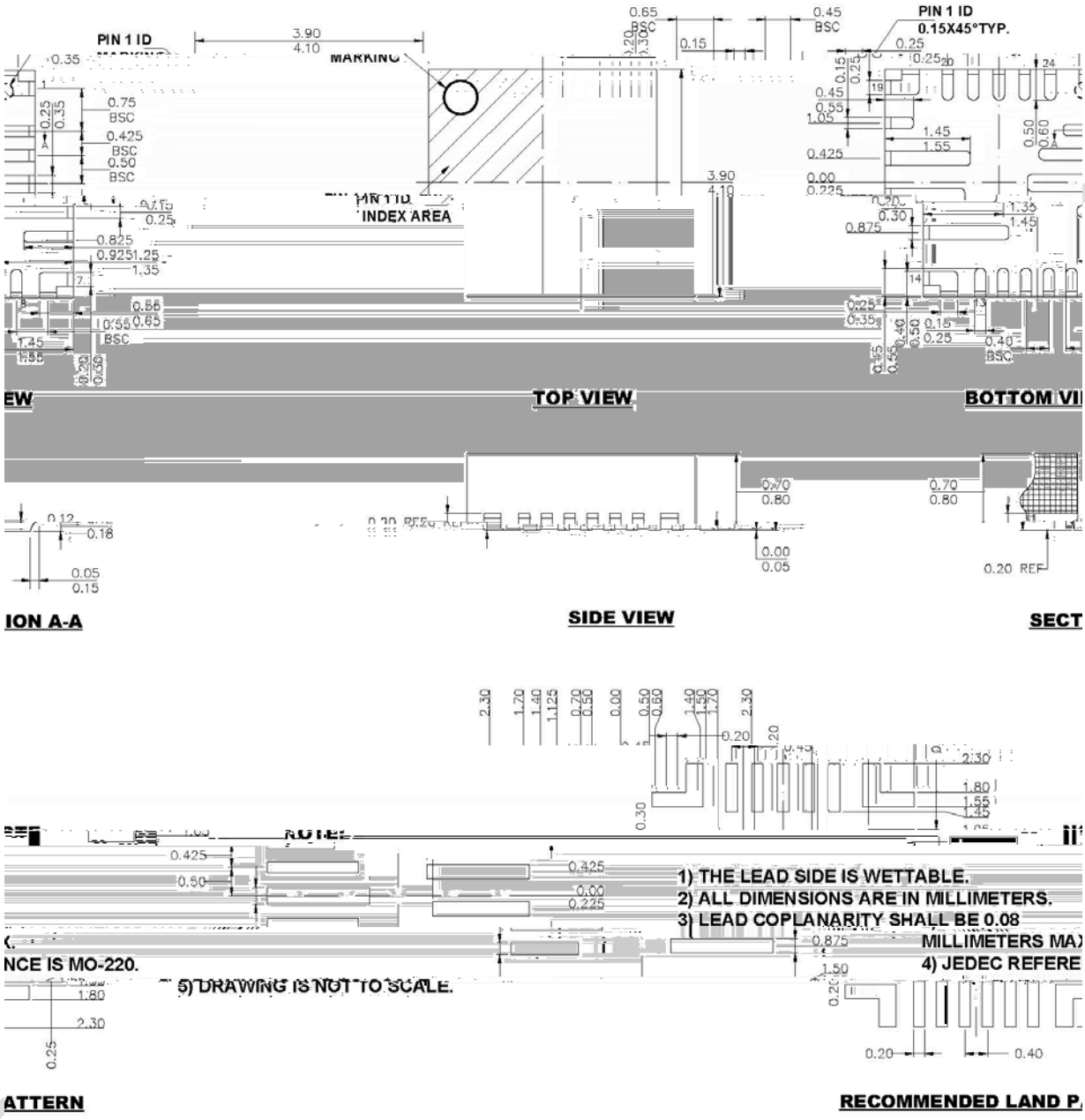
PACKAGE INFORMATION



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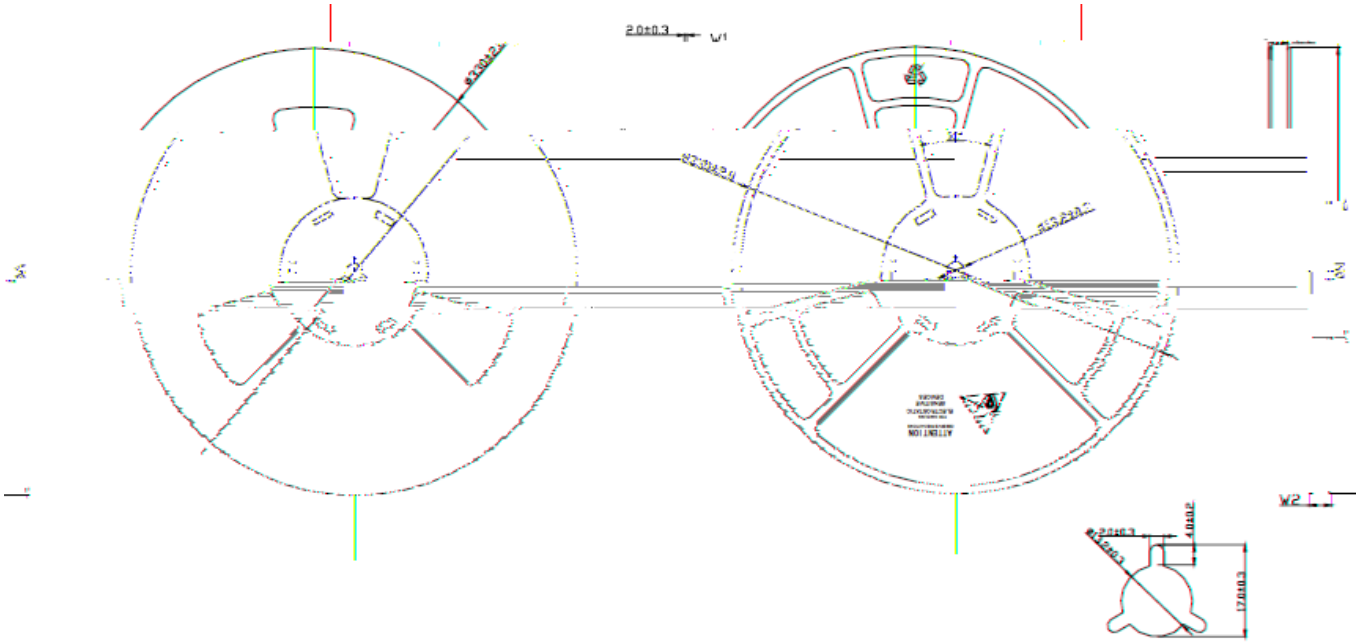
TAPE AND REEL INFORMATION



PRODUCT SPECIFICATIONS				
TYPE WIDTH	ØA	ØN	W1 (Min)	W2 (Max)
12MM	330±2.0	100±1.0	12.4	19.4
16mm	330±2.0	100±1.0	16.4	23.4
24MM	330±2.0	100±1.0	24.4	31.4
32MM	330±2.0	100±1.0	32.4	39.4
44MM	330±2.0	100±1.0	44.4	51.4

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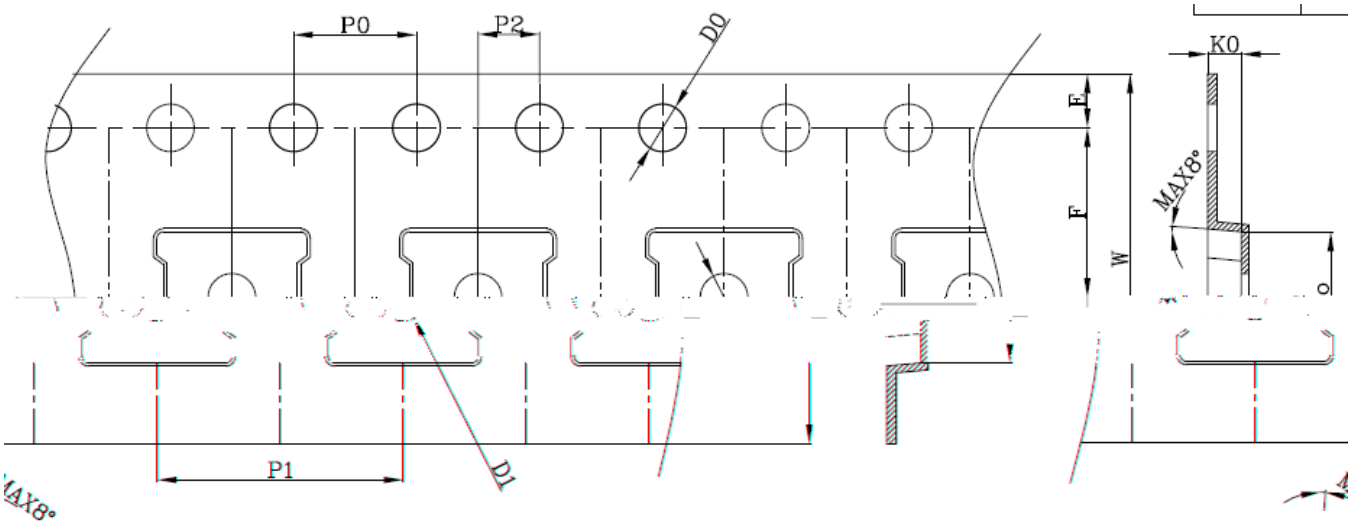

NOTE:
1. 材料:黑色防静电复合PS;
2. 10个链孔的累积公差不能超过
3. 250mm带子的扇形不得超过2
4. 所有尺寸符合EIA-481-B标准

SYMBOL	A0	B0	K0	P0	P1	P2
SPEC	4.00±0.10	8.00±0.10	2.00±0.05	4.30±0.10	4.30±0.10	1.10±0.10
SYMBOL	D0	D1	W	T	E	F
SPEC	1.55±0.05	1.55±0.10	12.00±0.30	0.30±0.05	1.75±0.10	5.50±0.05

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